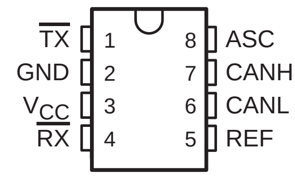
- **SN75LBC031 Meets Standard ISO/DIS 11898 (up to 500 k Baud)**
- **Driver Output Capability at 50 mA**
- **Wide Positive and Negative Input/output Bus Voltage Range**
- **Bus Outputs Short-Circuit-Protected to Battery Voltage and Ground**
- **Thermal Shutdown**
- **Available in Q-Temp Automotive**
  - **HighRel Automotive Applications**
  - **Configuration Control/Print Support**
  - **Qualification to Automotive Standards**

D PACKAGE
(TOP VIEW)



TERMINAL FUNCTIONS

TERMINAL	DESCRIPTION
$\overline{TX}$	Transmitter input
GND	Ground
V_{CC}	Supply voltage
$\overline{RX}$	Receiver output
REF	Reference output
CANL	Low side bus output driver
CANH	High side bus output driver
ASC	Adjustable slope control

FUNCTION TABLE

$\overline{TX}$	CANH	CANL	BUS STATE	$\overline{RX}$
L	H	L	Dominant	L
High or floating	Floating	Floating	Recessive	H

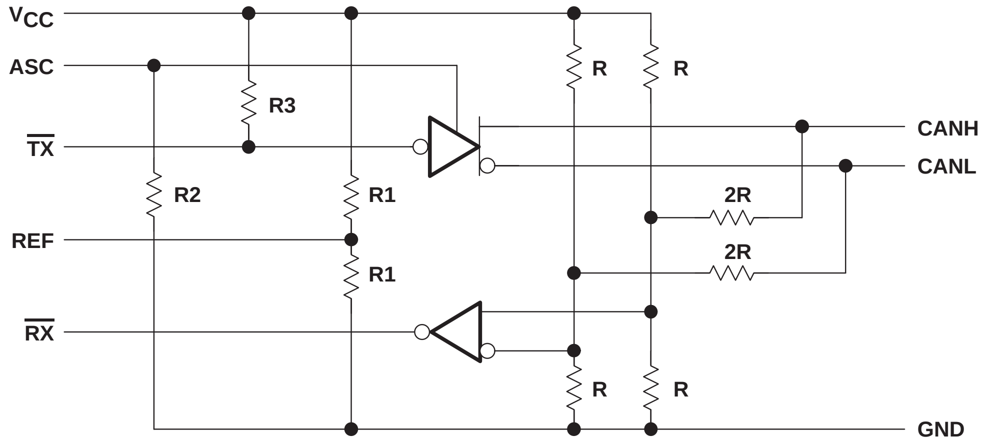
L = low, H = high

description

The SN75LBC031 is a CAN transceiver used as an interface between a CAN controller and the physical bus for high speed applications of up to 500 kBaud. The device provides transmit capability to the differential bus and differential receive capability to the controller. The transmitter outputs (CANH and CANL), feature internal transition regulation to provide controlled symmetry resulting in low EMI emissions. Both transmitter outputs are fully protected against battery short circuits and electrical transients that can occur on the bus lines. In the event of excessive device power dissipation the output drivers are disabled by the thermal shutdown circuitry at a junction temperature of approximately 160°C. The inclusion of an internal pullup resistor on the transmitter input ensures a defined output during power up and protocol controller reset. For normal operation at 500 kBaud the ASC terminal is open or tied to GND. For slower speed operation at 125 kBaud the bus output transition times can be increased to reduce EMI by connecting the ASC terminal to V_{CC}. The receiver includes an integrated filter that suppresses the signal into pulses less than 30 ns wide.

The SN75LBC031 is characterized for operation from –40°C to 85°C. The SN65LBC031 is characterized for operation from –40°C to 125°C. The SN65LBC031Q is characterized for operation over the automotive temperature range of –40°C to 125°C.

logic diagram



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Logic supply voltage, V_{CC} (see Note 1) . . . . 7 V
Bus terminal voltage . . . . –5 V to 20 V
Input current at $\overline{TX}$ and ASC terminal, I_I . . . . ±10 mA
Input voltage at $\overline{TX}$ and ASC terminal, V_I . . . . $2 \times V_{CC}$
Operating free-air temperature range, T_A: SN65LBC031, SN65LBC031Q . . . . –40°C to125°C
SN75LBC031 . . . . –40°C to 85°C
Operating juncation range, T_J . . . . –40°C to 150°C
Continuous total power dissipation at (or below) 25°C free-air temperature . . See Dissipation Rating Table
Storage temperature range, T_{stg} . . . . –65°C to 150°C
Case temperature for 10 sec T_C, D package . . . . 260°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage values, except differential bus voltage, are measured with respect to GND.

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$ POWER RATING	OPERATING FACTOR ABOVE T_C = 25°C	T_C = 125°C POWER RATING
D	725 mW	5.8 mW/°C	145 mW

DISSIPATION DERATING CURVE vs FREE-AIR TEMPERATURE

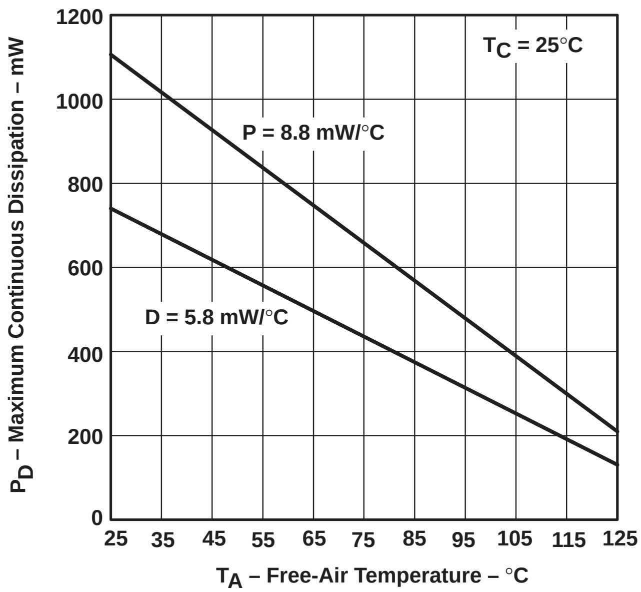


Figure 1

recommended operating conditions

		MIN	NOM	MAX	UNIT
Logic supply voltage, V_{CC}		4.5	5	5.5	V
Voltage at any bus terminal (separately or common mode), V_I or V_{IC} (see Note 3)		–2		7	V
High-level input voltage, V_{IH}	$\overline{TX}$	2		V_{CC}	V
Low-level input voltage, V_{IL}	$\overline{TX}$	0		0.8	V
High-level output current, I_{OH}	Transmitter			–50	mA
	Receiver			–400	µA
Low-level output current, I_{OL}	Transmitter			50	mA
	Receiver			1	
Operating free-air temperature, T_A	SN75LBC031	–40		85	°C
	SN65LBC031, SN65LBC031Q	–40		125	

NOTES: 2. All voltage values, except differential bus voltage, are measured with respect to the ground terminal.
3. For bus voltages from –5 V to –2 V and 7 V to 20 V the receiver output is stable.

SYMBOL DEFINITION

DATA SHEET PARAMETER	DEFINITION
$V_{O(CANHR)}$	CANH bus output voltage (recessive state)
$V_{O(CANLR)}$	CANL bus output voltage (recessive state)
$V_{O(CANHD)}$	CANH bus output voltage (dominant state)
$V_{O(CANLD)}$	CANL bus output voltage (dominant state)
$V_{O(DIFFR)}$	Bus differential output voltage (recessive state)
$V_{O(DIFFD)}$	Bus differential output voltage (dominant state)
$V_{I(ASC)}$	Adjustable slope control input voltage

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{O(REF)}$	Reference source output voltage	$I_{REF} = \pm 20\ \mu A$	$0.45 V_{CC}$		$0.55 V_{CC}$	V
$R_{O(REF)}$	Reference source output resistance		5		10	kΩ
$I_{CC(REC)}$	Logic supply current, recessive state	See Figure 2, S1 closed		12	20	mA
$I_{CC(DOM)}$	Logic supply current, dominant state			55	80	

transmitter electrical characteristics over recommended ranges of supply and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{O(CANHR)}$ $V_{O(CANLR)}$	Output voltage (recessive state)	See Figure 2, S1 open	2	$0.5V_{CC}$	3	V
$V_{O(DIFFR)}$	Differential output voltage (recessive state)		–500	0	50	mV
$V_{O(CANHD)}$	Output voltage (dominant state)	See Figure 2, S1 closed	2.75	3.5	4.5	V
$V_{O(CANLD)}$	Output voltage (dominant state)		0.5	1.5	2.25	
$V_{O(DIFFD)}$	Differential output voltage (dominant state)		1.5	2	3	
$I_{IH(TX)}$	High-level input current (TX)	V_{IH} = 2.4 V		–100	–185	µA
		$V_{IH} = V_{CC}$			±2	
$I_{IH(ASC)}$	High-level input current (ASC)	V_{IH} = 2.4 V		100	165	µA
		$V_{IH} = V_{CC}$		200	340	
$I_{IL(TX)}$	Low-level input current ($\overline{TX}$)	V_{IL} = 0.4 V		–180	–400	µA
$I_{IL(ASC)}$	Low-level input current (ASC)	V_{IL} = 0.4 V		15	25	µA
$C_{I(TX)}$	$\overline{TX}$ input capacitance			8		pF
$I_{O(ssH)}$	CANH short circuit output current	$V_{O(CANH)}$ = –2 V to 20 V		–95	–200	mA
$I_{O(ssL)}$	CANL short circuit output current	$V_{O(CANL)}$ = 20 V to –2 V		140	250	mA

NOTE 2: All voltage values, except differential bus voltage, are measured with respect to the ground terminal.

transceiver dynamic characteristics over recommended operating free-air temperature range and V_{CC} = 5 V

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
$t_{(loop)}$	Loop time	See Figures 2 and 3, S1 closed,	$V_{I(ASC)}$ = 0 V or open circuit, S2 open			280	ns
		See Figures 2 and 3, S1 closed,	$V_{I(ASC)} = V_{CC}$, S2 closed			400	ns
$SR_{(RD)}$	Differential-output slew rate (recessive to dominant)	See Figures 2 and 4, S1 closed,	$V_{I(ASC)}$ = 0 or open circuit, S2 open		35		V/µs
		See Figures 2 and 4, S1 closed,	$V_{I(ASC)} = V_{CC}$, S2 closed		10		V/µs
$SR_{(DR)}$	Differential-output slew rate (dominant to recessive)	See Figures 2 and 4, S1 closed,	$V_{I(ASC)}$ = 0 or open circuit, S2 open		10		V/µs
		See Figures 2 and 4, S1 closed,	$V_{I(ASC)} = V_{CC}$, S2 closed		10		V/µs
$t_{d(RD)}$	Differential-output delay time	See Figure 2,	S1 closed		55		ns
$t_{d(DR)}$					160		ns
$t_{pd(RECRD)}$	Receiver propagation delay time	See Figures 2 and 5			90		ns
$t_{pd(RECDR)}$					55		ns

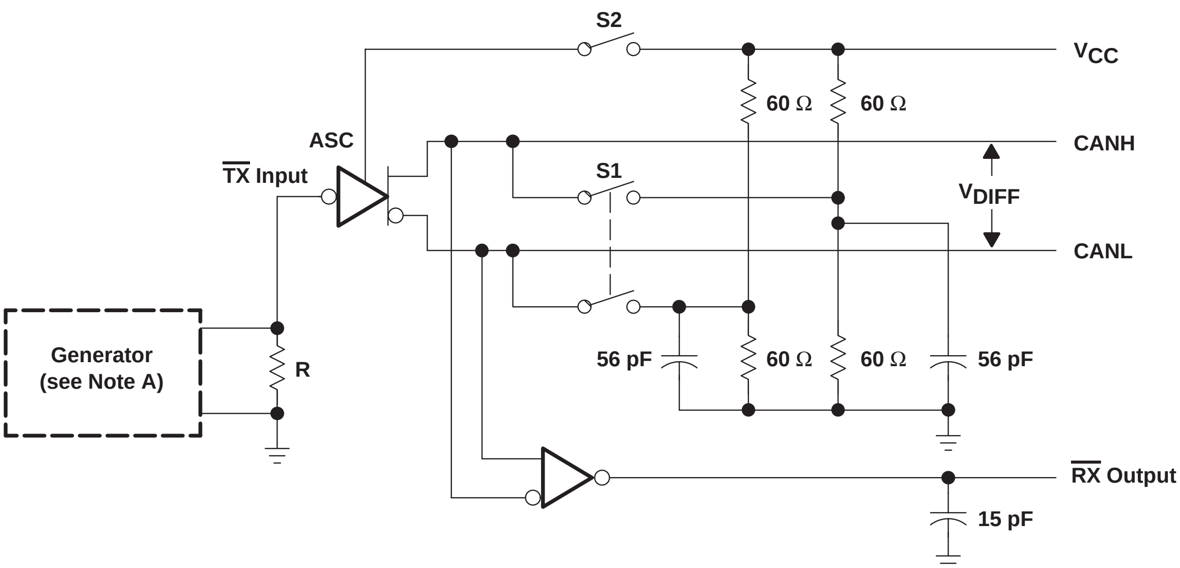
NOTE 4: Receiver input pulse width should be >50 ns. Input pulses of <30 ns are suppressed.

receiver electrical characteristics over recommended ranges of common-mode input voltage, supply voltage, and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{IT(REC)}$	Differential input threshold voltage for recessive state	V_{IC} = –2 V to 7 V			500	mV
$V_{IT(DOM)}$	Differential input threshold voltage for dominant state		900			
V_{hys}	Recessive-dominant input hysteresis		100	180		mV
$V_{OH(RX)}$	High-level output voltage	$V_{O(DIFF)}$ = 500 mV, I_{OH} = –400 µA	V_{CC}–0.5 V		V_{CC}	V
$V_{OL(RX)}$	Low-level output voltage	$V_{O(DIFF)}$ = 900 mV, I_{OL} = 1 mA	0		0.5	V
$r_{I(REC)}$	CANH and CANL input resistance in recessive state	dc, no load	5		50	kΩ
$r_{I(DIFF)}$	Differential CANH and CANL input resistance in recessive state	dc, no load	10		100	kΩ
C_i	CANH and CANL input capacitance			20		pF
$C_{i(DHL)}$	Differential CANH and CANL input capacitance			10		pF

NOTE 2: All voltage values, except differential bus voltage, are measured with respect to the ground terminal.

PARAMETER MEASUREMENT INFORMATION



NOTE A: The input pulse is supplied to $\overline{TX}$ by a generator having a t_r and t_f = 5 ns.

Figure 2. Test Circuit

PARAMETER MEASUREMENT INFORMATION

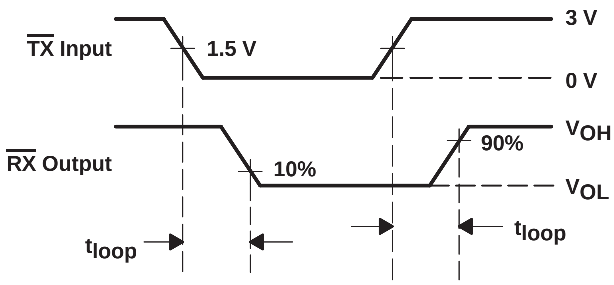


Figure 3. Loop Time

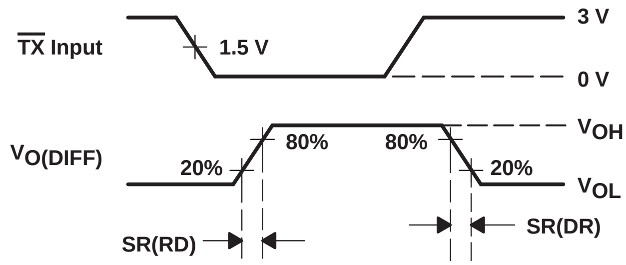
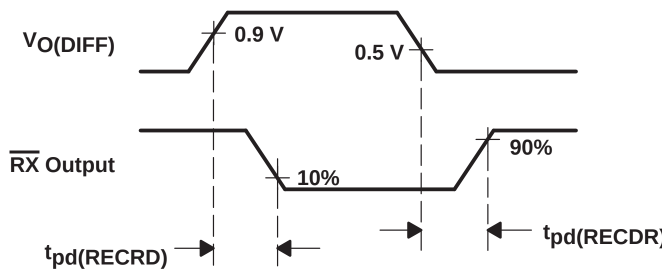


Figure 4. Slew Rate

NOTE A: The input pulse is supplied to $\overline{TX}$ by a generator having a t_r and t_f = 5 ns.



NOTE A: The input pulse is supplied as V_{DIFF} using CANH and CANL respectively by a generator having a t_r and t_f = 5 ns.

Figure 5. Receiver Delay Times

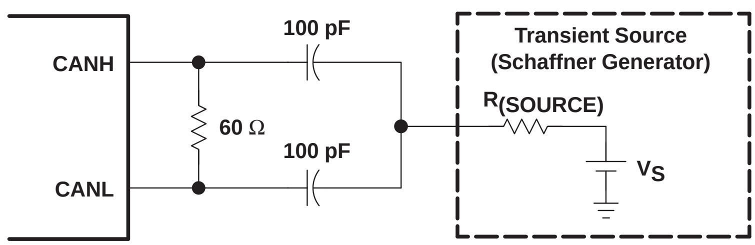


Figure 6. Transient Stress Capability Test Circuit

PARAMETER MEASUREMENT INFORMATION

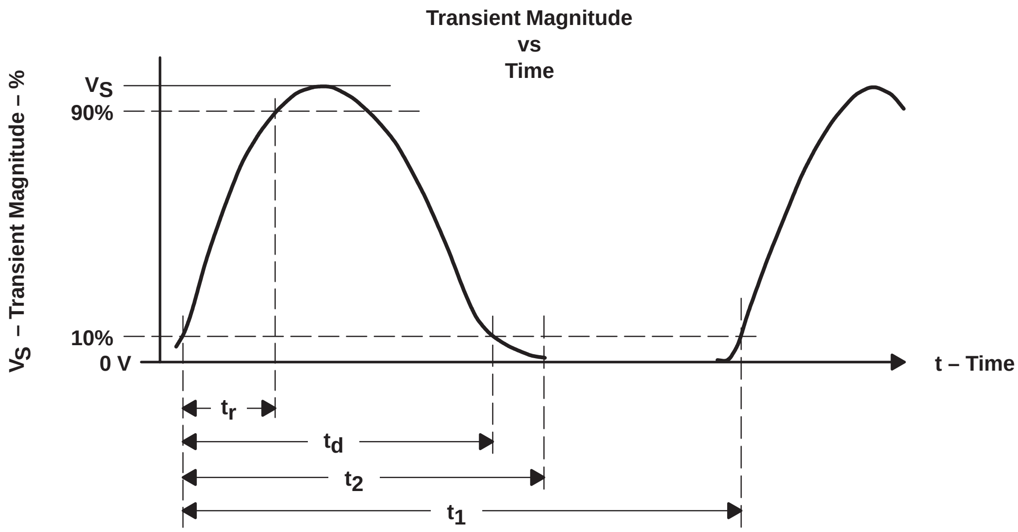


Figure 7. Transient Stress Capability Waveform

Table 1. Test Circuit Results According to DIN 40839

TEST PULSE	TRANSIENT MAGNITUDE V_S	SOURCE IMPEDANCE R_{SOURCE}	PULSE WIDTH t_d (see Note 5)	PULSE RISE TIME, t_r (see Note 6)	PULSE TIME, t_2 (see Figure 7)	REPETITION PERIOD, t_1 (see Figure 7)	NUMBER OF PULSES
1	–100 V	10 Ω	2 ms	1 µs	200 ms	5 s	5000
2	100 V	10 Ω	50 µs	1 µs	200 ms	5 s	5000
3a	–150 V	50 Ω	0.1 µs	5 ns	100 µs	100 µs	See Note 7
3b	100 V	50 Ω	0.1 µs	5 ns	100 µs	100 µs	See Note 7
5	60 V	1 Ω	400 ms	5 ms	—	—	1

NOTES: 5. Measured from 10% on rising edge to 10% on falling edge
6. Measured from 10% to 90% of pulse
7. Pulse package for a period of 3600 s, 10 ms pulse time, 90 ms stop time

SLRS048A – MAY 1998 – REVISED APRIL 2000

APPLICATION INFORMATION

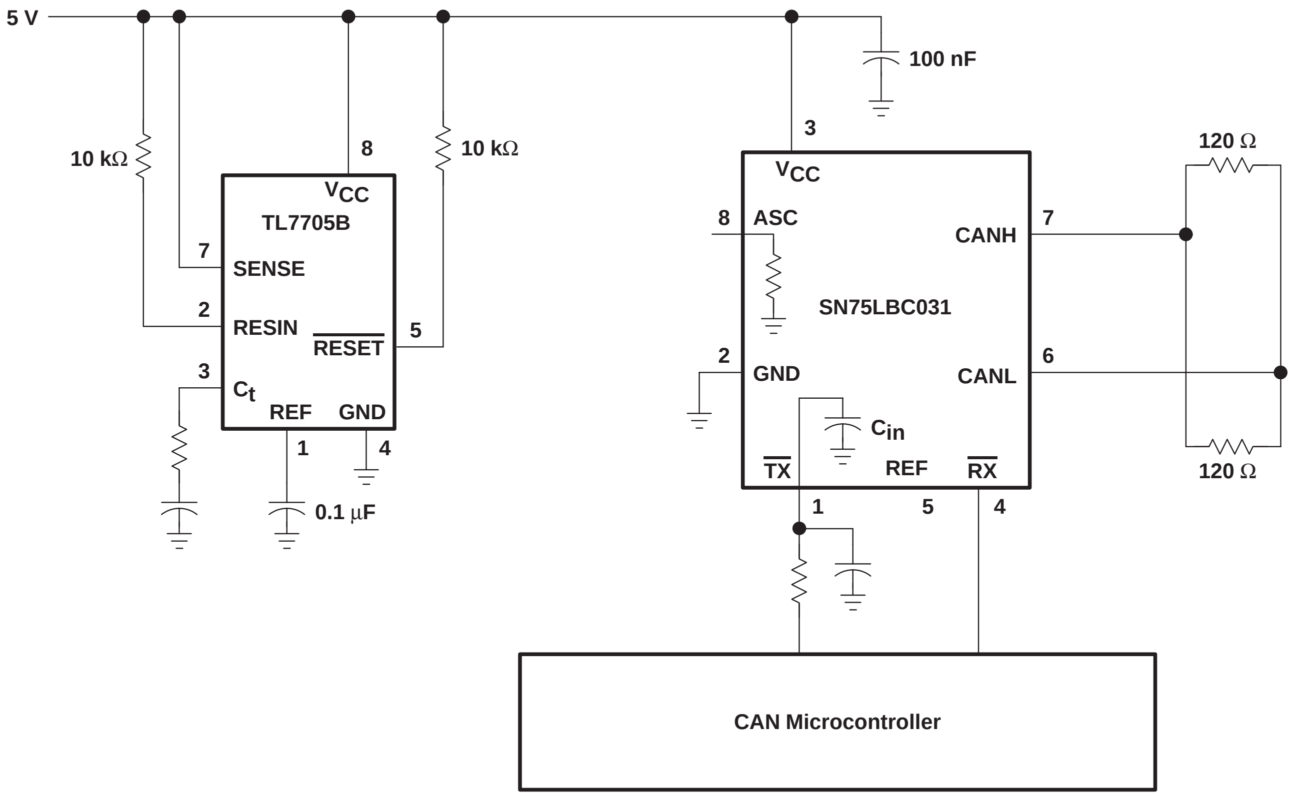
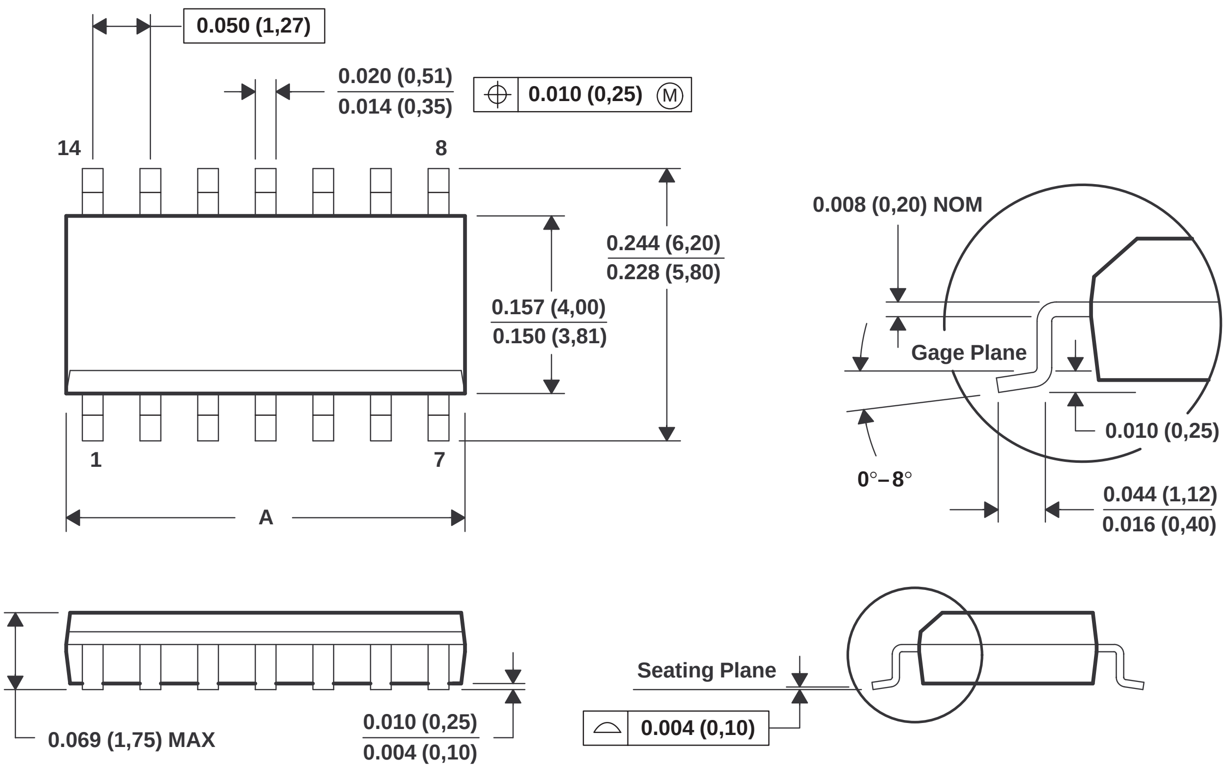


Figure 8. Typical SN75LBC031 Application

MECHANICAL DATA

D (R-PDSO-G)** **PLASTIC SMALL-OUTLINE PACKAGE**

14 PIN SHOWN



PINS ** / DIM	8	14	16
A MAX	0.197 (5,00)	0.344 (8,75)	0.394 (10,00)
A MIN	0.189 (4,80)	0.337 (8,55)	0.386 (9,80)

4040047 / D 10/96

NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion, not to exceed 0.006 (0,15).
D. Falls within JEDEC MS-012

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN65LBC031D	ACTIVE	SOIC	D	8	75	TBD	CU NIPDAU	Level-1-220C-UNLIM	-40 to 85	6LB031	Samples
SN65LBC031DG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	6LB031	Samples
SN65LBC031DRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM		6LB031	Samples
SN65LBC031QD	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	6LB031Q	Samples
SN65LBC031QDG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	6LB031Q	Samples
SN65LBC031QDR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	LB031Q	Samples
SN65LBC031QDRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	LB031Q	Samples
SN75LBC031D	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	7LB031	Samples
SN75LBC031DR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	7LB031	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

[4] There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

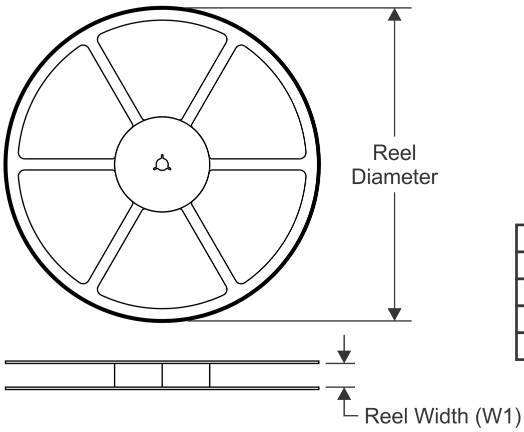
[5] Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

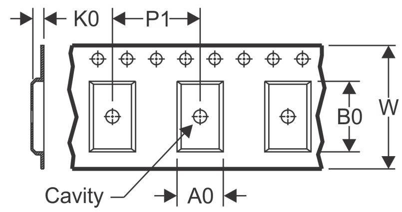
[6] Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

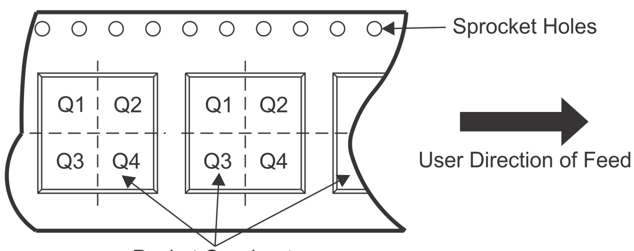
TAPE AND REEL INFORMATION





A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

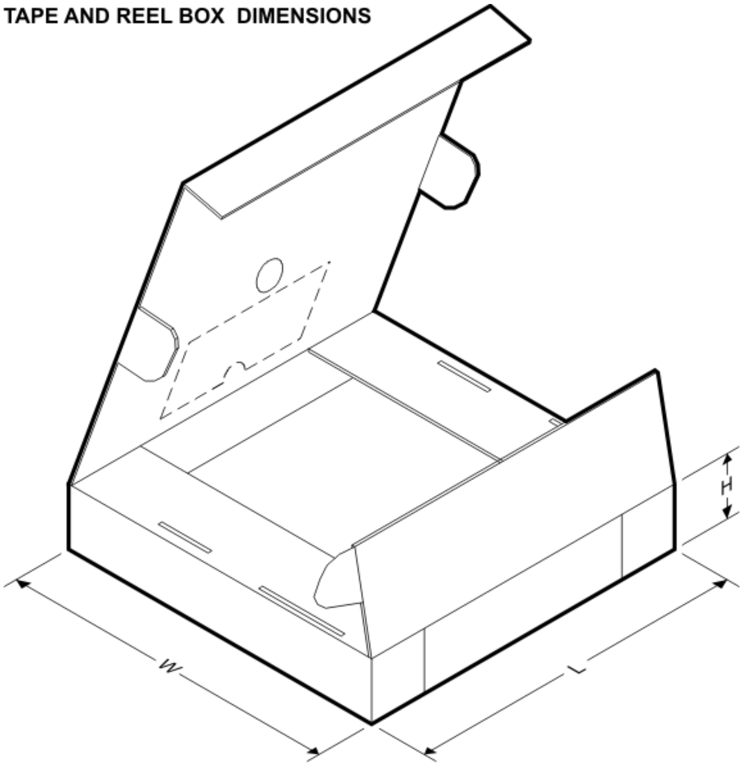
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN65LBC031QDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
SN65LBC031QDRG4	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
SN75LBC031DR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

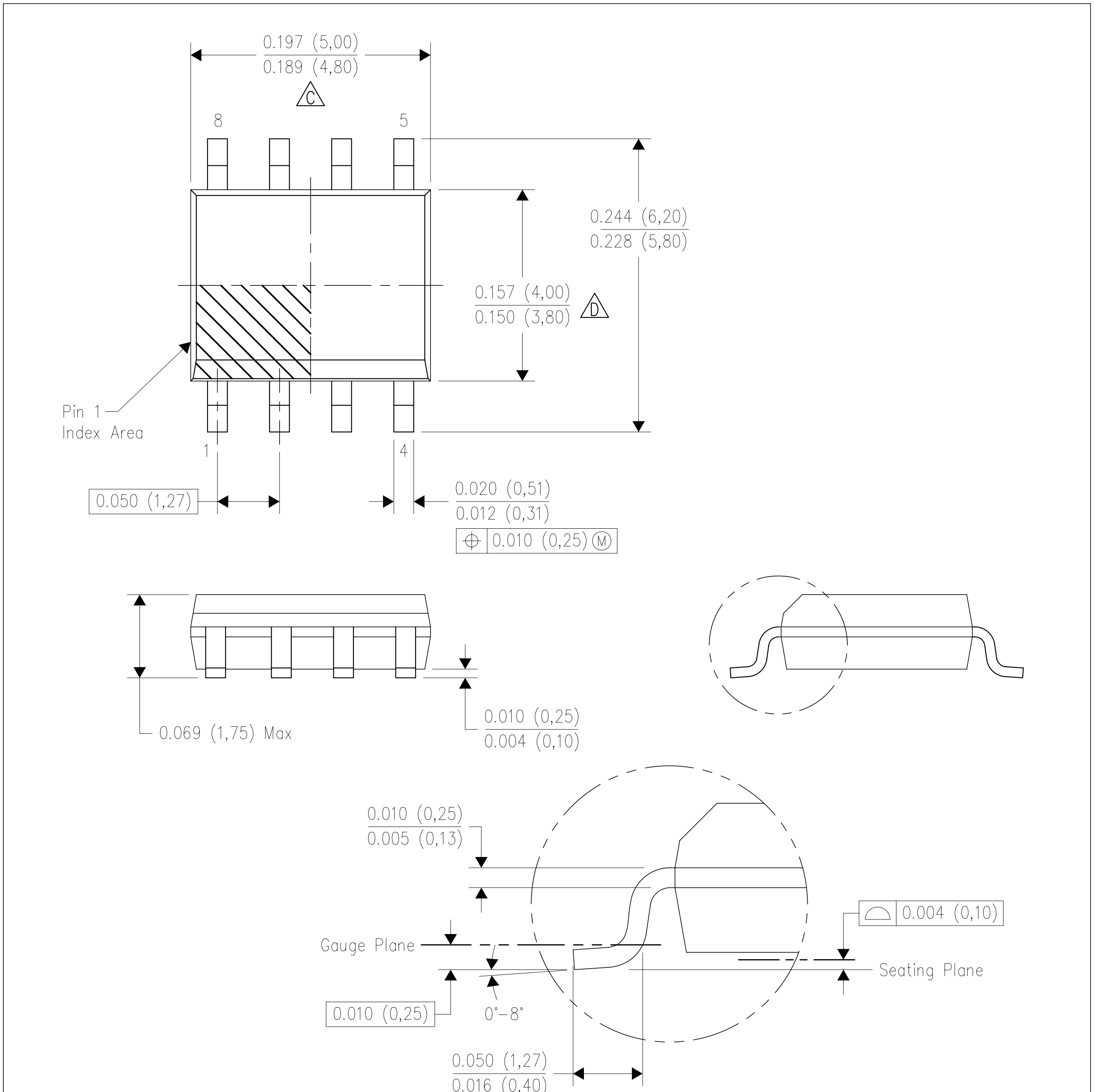
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN65LBC031QDR	SOIC	D	8	2500	367.0	367.0	38.0
SN65LBC031QDRG4	SOIC	D	8	2500	367.0	367.0	38.0
SN75LBC031DR	SOIC	D	8	2500	367.0	367.0	38.0

D (R–PDSO–G8) PLASTIC SMALL OUTLINE



4040047–3/M 06/11

NOTES:
- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
- D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
- E. Reference JEDEC MS-012 variation AA.

IMPORTANT NOTICE

Texas Instruments Incorporated (TI) reserves the right to make corrections, enhancements, improvements and other changes to its semiconductor products and services per JESD46, latest issue, and to discontinue any product or service per JESD48, latest issue. Buyers should obtain the latest relevant information before placing orders and should verify that such information is current and complete.

TI's published terms of sale for semiconductor products (http://www.ti.com/sc/docs/stdterms.htm) apply to the sale of packaged integrated circuit products that TI has qualified and released to market. Additional terms may apply to the use or sale of other types of TI products and services.

Reproduction of significant portions of TI information in TI data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. TI is not responsible or liable for such reproduced documentation. Information of third parties may be subject to additional restrictions. Resale of TI products or services with statements different from or beyond the parameters stated by TI for that product or service voids all express and any implied warranties for the associated TI product or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

Buyers and others who are developing systems that incorporate TI products (collectively, "Designers") understand and agree that Designers remain responsible for using their independent analysis, evaluation and judgment in designing their applications and that Designers have full and exclusive responsibility to assure the safety of Designers' applications and compliance of their applications (and of all TI products used in or for Designers' applications) with all applicable regulations, laws and other applicable requirements. Designer represents that, with respect to their applications, Designer has all the necessary expertise to create and implement safeguards that (1) anticipate dangerous consequences of failures, (2) monitor failures and their consequences, and (3) lessen the likelihood of failures that might cause harm and take appropriate actions. Designer agrees that prior to using or distributing any applications that include TI products, Designer will thoroughly test such applications and the functionality of such TI products as used in such applications.

TI's provision of technical, application or other design advice, quality characterization, reliability data or other services or information, including, but not limited to, reference designs and materials relating to evaluation modules, (collectively, "TI Resources") are intended to assist designers who are developing applications that incorporate TI products; by downloading, accessing or using TI Resources in any way, Designer (individually or, if Designer is acting on behalf of a company, Designer's company) agrees to use any particular TI Resource solely for this purpose and subject to the terms of this Notice.

TI's provision of TI Resources does not expand or otherwise alter TI's applicable published warranties or warranty disclaimers for TI products, and no additional obligations or liabilities arise from TI providing such TI Resources. TI reserves the right to make corrections, enhancements, improvements and other changes to its TI Resources. TI has not conducted any testing other than that specifically described in the published documentation for a particular TI Resource.

Designer is authorized to use, copy and modify any individual TI Resource only in connection with the development of applications that include the TI product(s) identified in such TI Resource. NO OTHER LICENSE, EXPRESS OR IMPLIED, BY ESTOPPEL OR OTHERWISE TO ANY OTHER TI INTELLECTUAL PROPERTY RIGHT, AND NO LICENSE TO ANY TECHNOLOGY OR INTELLECTUAL PROPERTY RIGHT OF TI OR ANY THIRD PARTY IS GRANTED HEREIN, including but not limited to any patent right, copyright, mask work right, or other intellectual property right relating to any combination, machine, or process in which TI products or services are used. Information regarding or referencing third-party products or services does not constitute a license to use such products or services, or a warranty or endorsement thereof. Use of TI Resources may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

TI RESOURCES ARE PROVIDED "AS IS" AND WITH ALL FAULTS. TI DISCLAIMS ALL OTHER WARRANTIES OR REPRESENTATIONS, EXPRESS OR IMPLIED, REGARDING RESOURCES OR USE THEREOF, INCLUDING BUT NOT LIMITED TO ACCURACY OR COMPLETENESS, TITLE, ANY EPIDEMIC FAILURE WARRANTY AND ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE, AND NON-INFRINGEMENT OF ANY THIRD PARTY INTELLECTUAL PROPERTY RIGHTS. TI SHALL NOT BE LIABLE FOR AND SHALL NOT DEFEND OR INDEMNIFY DESIGNER AGAINST ANY CLAIM, INCLUDING BUT NOT LIMITED TO ANY INFRINGEMENT CLAIM THAT RELATES TO OR IS BASED ON ANY COMBINATION OF PRODUCTS EVEN IF DESCRIBED IN TI RESOURCES OR OTHERWISE. IN NO EVENT SHALL TI BE LIABLE FOR ANY ACTUAL, DIRECT, SPECIAL, COLLATERAL, INDIRECT, PUNITIVE, INCIDENTAL, CONSEQUENTIAL OR EXEMPLARY DAMAGES IN CONNECTION WITH OR ARISING OUT OF TI RESOURCES OR USE THEREOF, AND REGARDLESS OF WHETHER TI HAS BEEN ADVISED OF THE POSSIBILITY OF SUCH DAMAGES.

Unless TI has explicitly designated an individual product as meeting the requirements of a particular industry standard (e.g., ISO/TS 16949 and ISO 26262), TI is not responsible for any failure to meet such industry standard requirements.

Where TI specifically promotes products as facilitating functional safety or as compliant with industry functional safety standards, such products are intended to help enable customers to design and create their own applications that meet applicable functional safety standards and requirements. Using products in an application does not by itself establish any safety features in the application. Designers must ensure compliance with safety-related requirements and standards applicable to their applications. Designer may not use any TI products in life-critical medical equipment unless authorized officers of the parties have executed a special contract specifically governing such use. Life-critical medical equipment is medical equipment where failure of such equipment would cause serious bodily injury or death (e.g., life support, pacemakers, defibrillators, heart pumps, neurostimulators, and implantables). Such equipment includes, without limitation, all medical devices identified by the U.S. Food and Drug Administration as Class III devices and equivalent classifications outside the U.S.

TI may expressly designate certain products as completing a particular qualification (e.g., Q100, Military Grade, or Enhanced Product). Designers agree that it has the necessary expertise to select the product with the appropriate qualification designation for their applications and that proper product selection is at Designers' own risk. Designers are solely responsible for compliance with all legal and regulatory requirements in connection with such selection.

Designer will fully indemnify TI and its representatives against any damages, costs, losses, and/or liabilities arising out of Designer's non-compliance with the terms and provisions of this Notice.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265