- **Perform Fixed-Rate or Variable-Rate Frequency Division**

- **For Applications in Arithmetic, Radar, Digital-to-Analog (D/A), Analog-to-Digital (A/D), and other Conversion Operations**

- **Typical Maximum Clock Frequency . . . 32 Megahertz**

```
              SN5497 . . . J PACKAGE
              SN7497 . . . N PACKAGE
                  (TOP VIEW)

              ┌──────────────┐
         B1 │ 1        16 │ V_CC
         B4 │ 2        15 │ B3
         B5 │ 3        14 │ B2
         B0 │ 4        13 │ CLR
          Z │ 5        12 │ UNITY/CAS
          Y │ 6        11 │ EN in
     EN out │ 7        10 │ STRB
        GND │ 8         9 │ CLK
              └──────────────┘
```

Rate Inputs: B1, B4, B5, B0 (left) — Rate Inputs: B3, B2 (right)

description

These monolithic, fully synchronous, programmable counters utilize Series 54/74 TTL circuitry to achieve 32-megahertz typical maximum operating frequencies. These six-bit serial binary counters feature buffered clock, clear, and enable inputs to control the operation of the counter, and a strobe input to enable or inhibit the rate input/decoding AND-OR-INVERT gates. The outputs have additional gating for cascading and transferring unity-count rates.

The counter is enabled when the clear, strobe, and enable inputs are low. With the counter enabled, the output frequency is equal to the input frequency multiplied by the rate input M and divided by 64, ie.:

$$f_{out} = \frac{M \cdot f_{in}}{64}$$

where: $M = F \cdot 2^5 + E \cdot 2^4 + D \cdot 2^3 + C \cdot 2^2 + B \cdot 2^1 + A \cdot 2^0$

When the rate input is binary 0 (all rate inputs low), Z remains high. In order to cascade devices to perform 12-bit rate multiplication, the enable output is connected to the enable and strobe inputs of the next stage, the Z output of each stage is connected to the unity/cascade input of the other stage, and the sub-multiple frequency is taken from the Y output.
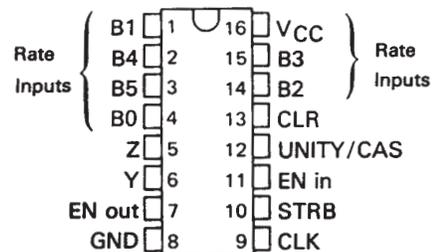
The unity/cascade input, when connected to the clock input, may be utilized to pass the clock frequency (inverted) to the Y output when the rate input/decoding gates are inhibited by the strobe. The unity/cascade input may also be used as a control for the Y output.

logic symbol[†]
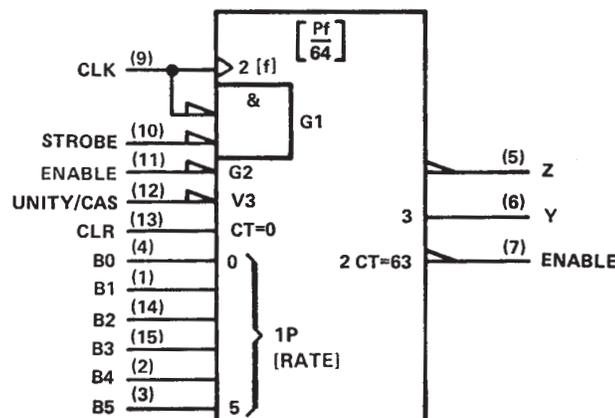
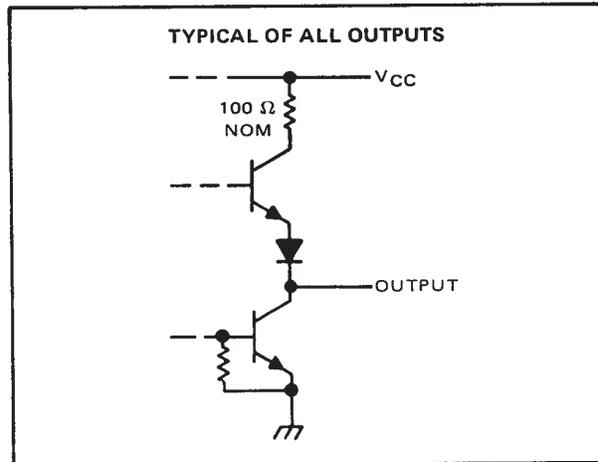[†] This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
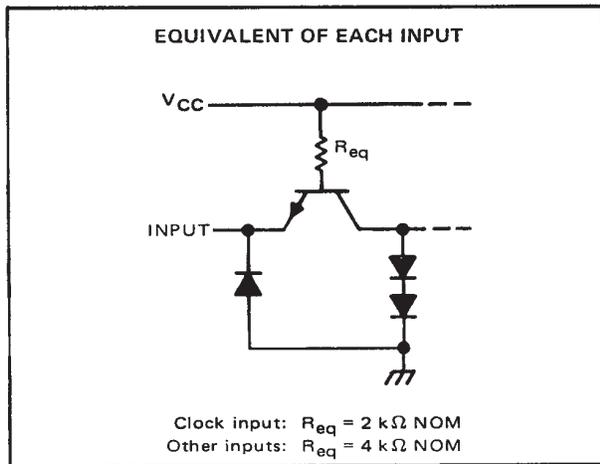

TEXAS INSTRUMENTS

schematics of inputs and outputs

EQUIVALENT OF EACH INPUT	TYPICAL OF ALL OUTPUTS
Clock input: $R_{eq} = 2 \text{ k}\Omega$ NOM Other inputs: $R_{eq} = 4 \text{ k}\Omega$ NOM	

STATE AND/OR RATE FUNCTION TABLE (See Note A)

	INPUTS						OUTPUTS			
			BINARY RATE			LOGIC LEVEL OR NUMBER OF PULSES			
CLEAR	ENABLE	STROBE	B5 B4 B3 B2 B1 B0	NUMBER OF CLOCK PULSES	UNITY/ CASCADE	Y	Z	ENABLE	NOTES
H	X	H	X X X X X X	X	H	L	H	H	B
L	L	L	L L L L L L	64	H	L	H	1	C
L	L	L	L L L L L H	64	H	1	1	1	C
L	L	L	L L L L H L	64	H	2	2	1	C
L	L	L	L L L H L L	64	H	4	4	1	C
L	L	L	L L H L L L	64	H	8	8	1	C
L	L	L	L H L L L L	64	H	16	16	1	C
L	L	L	H L L L L L	64	H	32	32	1	C
L	L	L	H H H H H H	64	H	63	63	1	C
L	L	L	H H H H H H	64	L	H	63	1	D
L	L	L	H L H L L L	64	H	40	40	1	E

NOTES: A. H = high level, L = low level, X = irrelevant. All remaining entries are numeric counts.
   B. This is a simplified illustration of the clear function. The states of clock and strobe can affect the logic level of Y and Z. A low unity/cascade will cause output Y to remain high.
   C. Each rate illustrated assumes a constant value at rate inputs; however, these illustrations in no way prohibit variable-rate inputs.
   D. Unity/cascade is used to inhibit output Y.
   E. $f_{out} = \dfrac{M \cdot f_{in}}{64} = \dfrac{(8 + 32) f_{in}}{64} = \dfrac{40 f_{in}}{64} = 0.625 f_{in}$

TEXAS INSTRUMENTS
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logic diagram (positive logic)
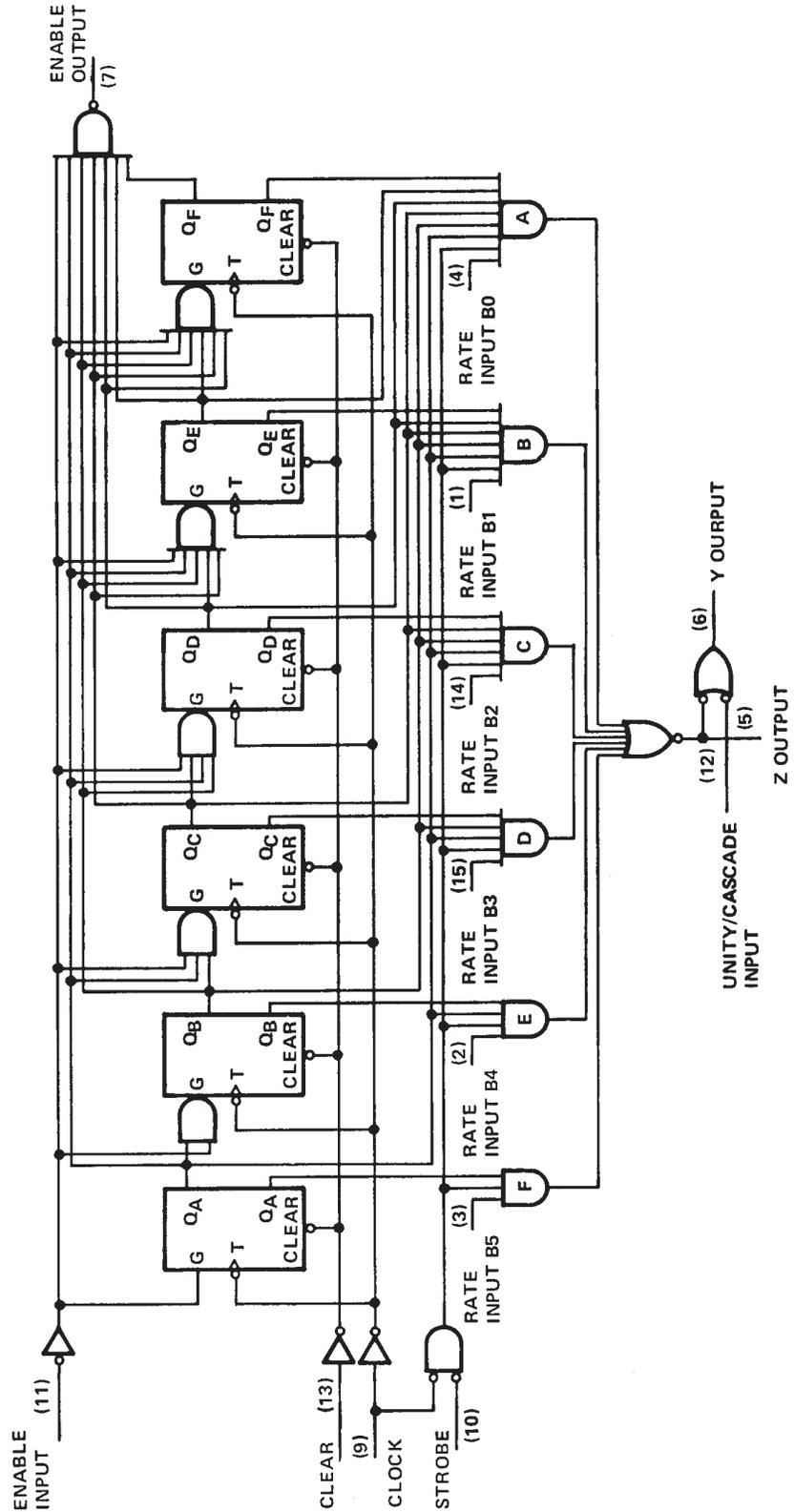
SN5497, SN7497
SYNCHRONOUS 6-BIT BINARY RATE MULTIPLIERS

SDLS130 – DECEMBER 1972 – REVISED MARCH 1988

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . 7 V
Input voltage . . . . 5.5 V
Operating free-air temperature range: SN5497 (see Note 2) . . . . −55°C to 125°C
SN7497 . . . . 0°C to 70°C
Storage temperature range . . . . −65°C to 150°C

recommended operating conditions

		SN5497			SN7497			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}		4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}				−400			−400	μA
Low-level output current, I_{OL}				16			16	mA
Clock frequency, f_{clock}		0		25	0		25	MHz
Width of clock pulse, $t_{w(clock)}$		20			20			ns
Width of clear pulse, $t_{w(clear)}$		15			15			ns
Enable setup time, t_{su}:	(See Figure 1)							ns
Before positive-going transition of clock pulse		25			25			
Before negative-going transition of previous clock pulse		0		$t_{w(clock)}$−10	0		$t_{w(clock)}$−10	
Enable hold time, t_h:	(See Figure 1)							ns
After positive-going transition of clock pulse		0		$t_{w(clock)}$−10	0		$t_{w(clock)}$−10	
After negative-going transition of previous clock pulse		20		t_{cp}−10	20		t_{cp}−10	
Operating free-air temperature, T_A (See Note 2)		−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS[†]		MIN	TYP[‡]	MAX	UNIT
V_{IH}	High-level input voltage			2			V
V_{IL}	Low-level input voltage					0.8	V
V_{IK}	Input clamp voltage	V_{CC} = MIN,	I_I = −12 mA			−1.5	V
V_{OH}	High-level output voltage	V_{CC} = MIN, V_{IL} = 0.8 V,	V_{IH} = 2 V, I_{OH} = −400 μA	2.4	3.4		V
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{IL} = 0.8 V,	V_{IH} = 2 V, I_{OL} = 16 mA		0.2	0.4	V
I_I	Input current at maximum input voltage	V_{CC} = MAX,	V_I = 5.5 V			1	mA
I_{IH}	High-level input current	clock input	V_{CC} = MAX,	V_I = 2.4 V			80	μA
		other inputs					40	
I_{IL}	Low-level input current	clock input	V_{CC} = MAX,	V_I = 0.4 V			−3.2	mA
		other inputs					−1.6	
I_{OS}	Short circuit output current[§]	V_{CC} = MAX		−18		−55	mA
I_{CCH}	Supply current, outputs high	V_{CC} = MAX,	See Note 3		58		mA
I_{CCL}	Supply current, outputs low	V_{CC} = MAX,	See Note 4		80	120	mA

[†]For test conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
[‡]All typical values are at V_{CC} = 5 V, T_A = 25°C.
[§]Not more than one output should be shorted at a time.
NOTES: 1. Voltage values are with respect to network ground terminal.
2. An SN5497 in the W package operating at free-air temperatures above 118°C requires a heat sink that provides a thermal resistance from case to free-air, $R_{\theta CA}$, of not more than 55°C/W.
3. I_{CCH} is measured with outputs open and all inputs grounded.
4. I_{CCL} is measured with outputs open and all inputs at 4.5 V.

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switching characteristics, $V_{CC} = 5$ V, $T_A = 25°C$, N = 10

| PARAMETER[†]	FROM INPUT	TO OUTPUT	TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{max}				25	32		MHz
t_{PLH}	Enable	Enable			13	20	ns
t_{PHL}					14	21	
t_{PLH}	Strobe	Z			12	18	ns
t_{PHL}					15	23	
t_{PLH}	Clock	Y			26	39	ns
t_{PHL}					20	30	
t_{PLH}	Clock	Z			12	18	ns
t_{PHL}					17	26	
t_{PLH}	Rate	Z	$C_L = 15$ pF, $R_L = 400$ Ω, See Figure 1		6	10	ns
t_{PHL}					9	14	
t_{PLH}	Unity/Cascade	Y			9	14	ns
t_{PHL}					6	10	
t_{PLH}	Strobe	Y			19	30	ns
t_{PHL}					22	33	
t_{PLH}	Clock	Enable			19	30	ns
t_{PHL}					22	33	
t_{PLH}	Clear	Y			24	36	ns
t_{PHL}		Z			15	23	
t_{PLH}	Any Rate Input	Y			15	23	ns
t_{PHL}					15	23	

[†]f_{max} ≡ maximum clock frequency.

t_{PLH} ≡ propagation delay time, low-to-high-level output.

t_{PHL} ≡ propagation delay time, high-to-low-level output.

TYPICAL APPLICATION DATA

This application demonstrates how the '97 can be cascaded to perform 18-bit rate multiplication. This scheme is expandable to n-bits by extending the pattern illustrated.
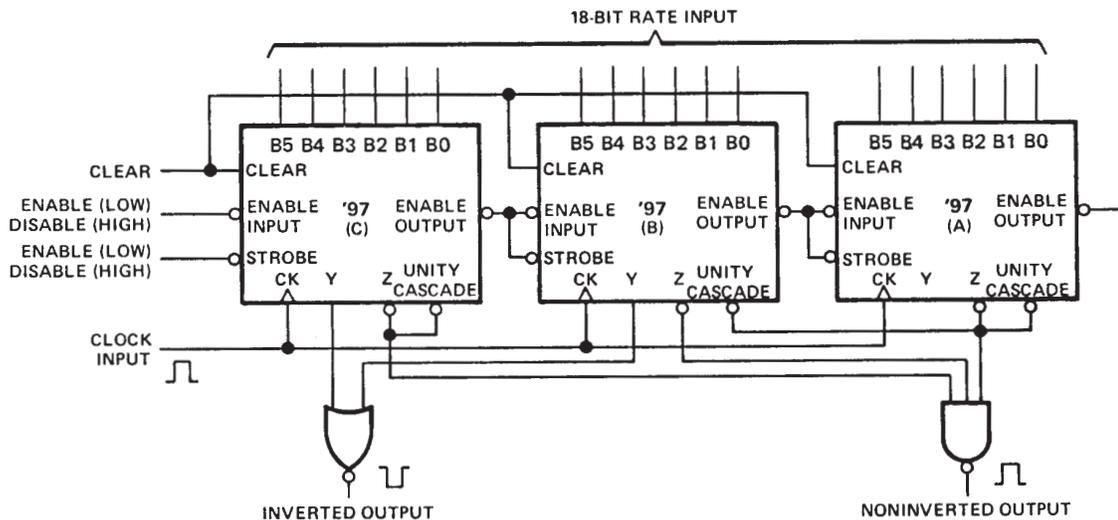

As illustrated, two of the 6-bit multipliers can be cascaded by connecting the Z output of unit A to the unity cascade input of unit B, in which case, a two-input NOR gate is used to cascade the remaining multipliers. Alternatively, all three Y outputs can be cascaded with a 3-input NOR gate. The three unused unity cascade inputs can be conveniently terminated by connecting each to its Z output.
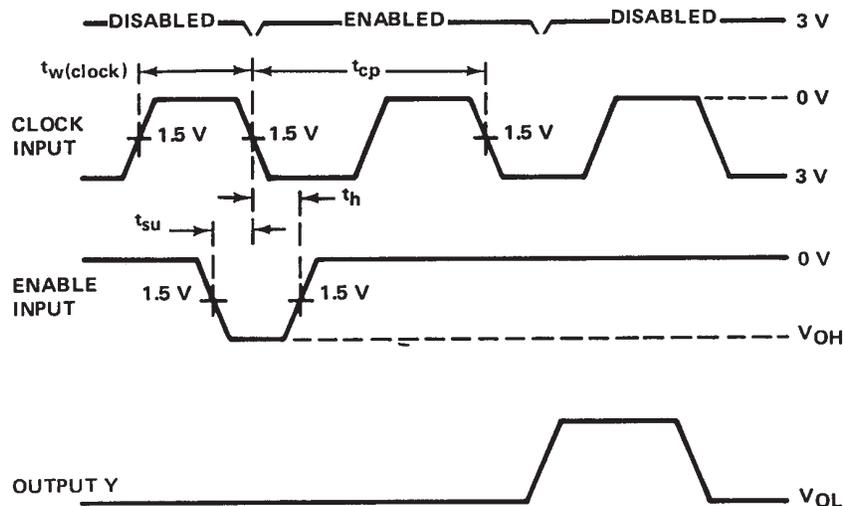
PARAMETER MEASUREMENT INFORMATION
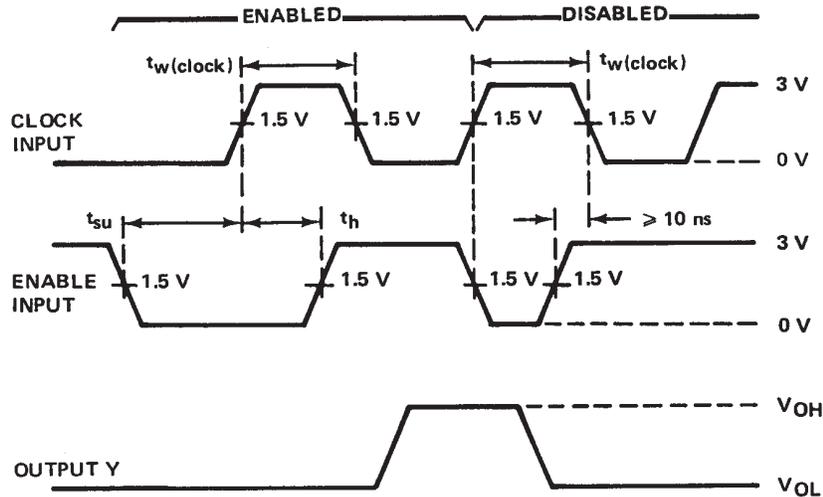
ENABLING FROM POSITIVE-GOING
TRANSITION OF CLOCK PULSE

ENABLING FROM NEGATIVE-GOING
TRANSITION OF PREVIOUS CLOCK PULSE

1. Unity/Cascade and pin 2 (rate input), other inputs are low. Clear the counter and apply clock and enable pulse as illustrated.
2. Setup and hold times are illustrated for enabling a single clock pulse (count). Continued application of the enable function will enable subsequent clock pulse (counts) until disabling occurs (enable goes high). The total number of counts will be determined by the total number of positive-going clock transition enabled.
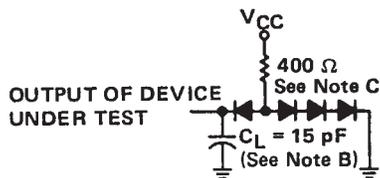
NOTES: A. The input pulse generator has the following characteristics: $t_{w(clock)} = 20$ ns, $t_{TLH} \leqslant 10$ ns, $t_{THL} \leqslant 10$ ns, PRR = 1 MHz, $Z_{out} \approx 50 \; \Omega$.
       B. C_L includes probe and jig capacitance.
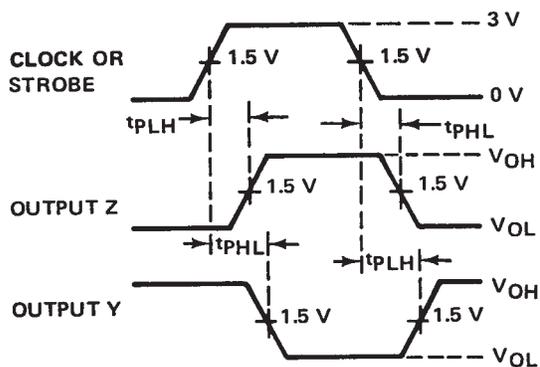   C. All diodes are 1N3064 or equivalent.

FIGURE 1—SWITCHING TIMES

![Texas Instruments logo]
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PARAMETER MEASUREMENT INFORMATION

All three outputs are loaded during testing.

LOAD CIRCUIT

Flip-flops are at a count so that all other inputs to the gate under test are high and all other inputs, including other rate inputs, are low.

**PROPAGATION DELAY TIMES,
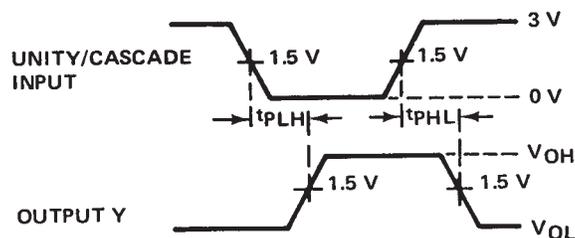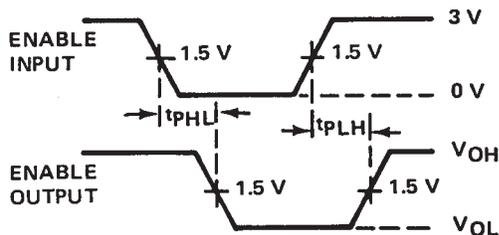RATE INPUT TO Z**

Unity/cascade and rate inputs are high, other inputs are low, and flip-flops are at any count other than maximum.

**PROPAGATION DELAY TIMES, CLOCK TO Z AND Y,
AND STROBE INPUT TO Z AND Y**

Output Z is high.

**PROPAGATION DELAY TIMES,
UNITY/CASCADE INPUT TO Y**

Flip-flops are at the maximum count. Other inputs are low.

**PROPAGATION DELAY TIMES,
ENABLE INPUT TO ENABLE OUTPUT**

NOTES: A. The input pulse generator has the following characteristics: $t_{w(clock)} = 20$ ns, $t_{TLH} \leqslant 10$ ns, $t_{THL} \leqslant 10$ ns, PRR = 1 MHz, $Z_{out} \approx 50\ \Omega$.
     B. C_L includes probe and jig capacitance.
     C. All diodes are 1N3064 or equivalent.

FIGURE 1—SWITCHING TIMES (CONTINUED)

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN5497J	ACTIVE	CDIP	J	16	1	TBD	A42	N / A for Pkg Type	-55 to 125	SN5497J	Samples
SN7497N	ACTIVE	PDIP	N	16	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	0 to 70	SN7497N	Samples
SN7497N	ACTIVE	PDIP	N	16	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	0 to 70	SN7497N	Samples
SN7497NE4	ACTIVE	PDIP	N	16	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	0 to 70	SN7497N	Samples
SN7497NE4	ACTIVE	PDIP	N	16	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	0 to 70	SN7497N	Samples
SNJ5497J	ACTIVE	CDIP	J	16	1	TBD	A42	N / A for Pkg Type	-55 to 125	SNJ5497J	Samples
SNJ5497J	ACTIVE	CDIP	J	16	1	TBD	A42	N / A for Pkg Type	-55 to 125	SNJ5497J	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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OTHER QUALIFIED VERSIONS OF SN5497, SN7497 :
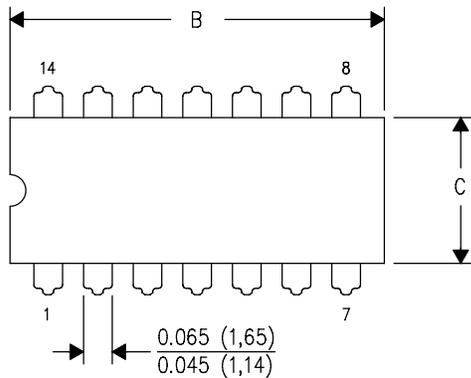
- Catalog: SN7497

- Military: SN5497

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product

- Military - QML certified for Military and Defense Applications

J (R−GDIP−T**) CERAMIC DUAL IN−LINE PACKAGE
14 LEADS SHOWN

DIM \ PINS **	14	16	18	20
A	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC
B MAX	0.785 (19,94)	.840 (21,34)	0.960 (24,38)	1.060 (26,92)
B MIN	——	——	——	——
C MAX	0.300 (7,62)	0.300 (7,62)	0.310 (7,87)	0.300 (7,62)
C MIN	0.245 (6,22)	0.245 (6,22)	0.220 (5,59)	0.245 (6,22)

B

14   8

1   7

$\frac{0.065 (1,65)}{0.045 (1,14)}$

C

0.005 (0,13) MIN

$\frac{0.060 (1,52)}{0.015 (0,38)}$

0.200 (5,08) MAX

Seating Plane

0.130 (3,30) MIN

$\frac{0.026 (0,66)}{0.014 (0,36)}$

0.100 (2,54)

A

0°−15°

$\frac{0.014 (0,36)}{0.008 (0,20)}$
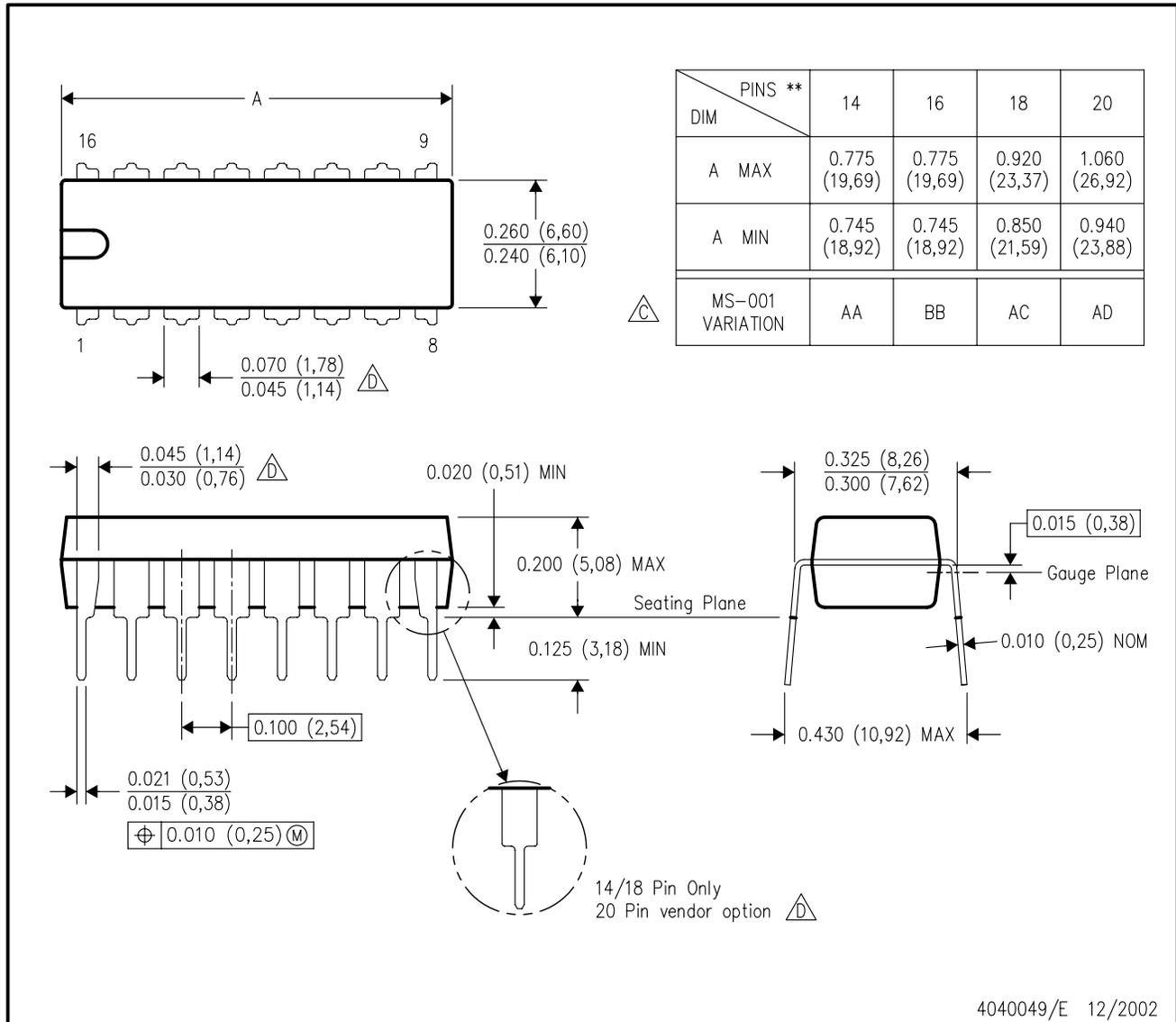
4040083/F 03/03

NOTES: A. All linear dimensions are in inches (millimeters).
        B. This drawing is subject to change without notice.
        C. This package is hermetically sealed with a ceramic lid using glass frit.
        D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
        E. Falls within MIL STD 1835 GDIP1−T14, GDIP1−T16, GDIP1−T18 and GDIP1−T20.

N (R−PDIP−T**)
16 PINS SHOWN

PLASTIC DUAL−IN−LINE PACKAGE

DIM \ PINS **	14	16	18	20
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
MS−001 VARIATION /C\	AA	BB	AC	AD

0.260 (6,60) / 0.240 (6,10)

0.070 (1,78) / 0.045 (1,14) /D\

0.045 (1,14) / 0.030 (0,76) /D\

0.020 (0,51) MIN

0.200 (5,08) MAX

Seating Plane

0.125 (3,18) MIN

0.100 (2,54)

0.021 (0,53) / 0.015 (0,38)

⊕ 0.010 (0,25) Ⓜ

14/18 Pin Only
20 Pin vendor option /D\

0.325 (8,26) / 0.300 (7,62)

0.015 (0,38)

Gauge Plane

0.010 (0,25) NOM

0.430 (10,92) MAX

4040049/E 12/2002

NOTES: A. All linear dimensions are in inches (millimeters).
   B. This drawing is subject to change without notice.
   /C\ Falls within JEDEC MS−001, except 18 and 20 pin minimum body length (Dim A).
   /D\ The 20 pin end lead shoulder width is a vendor option, either half or full width.

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