

551S

Low Skew 1 to 4 Clock Buffer

Description

The 551S is a low cost, high-speed single input to four output clock buffer with best in class additive phase jitter of sub 50fsec.

Renesas makes many non-PLL and PLL based low skew output devices as well as Zero Delay Buffers to synchronize clocks. Contact Renesas for all of your clocking needs.

Features

- Low additive phase jitter RMS: 50fs
- Extremely low skew outputs (50ps)
- Low cost clock buffer
- Packaged in 8-SOIC, 8-TSSOP, and 8-DFN
- Input/output clock frequency up to 200MHz
- Non-inverting output clock
- Ideal for networking clocks
- Operating voltages: 1.8V to 3.3V
- Output Enable mode tri-states outputs
- Advanced, low power CMOS process
- Extended temperature range (-40°C to +105°C)

Block Diagram

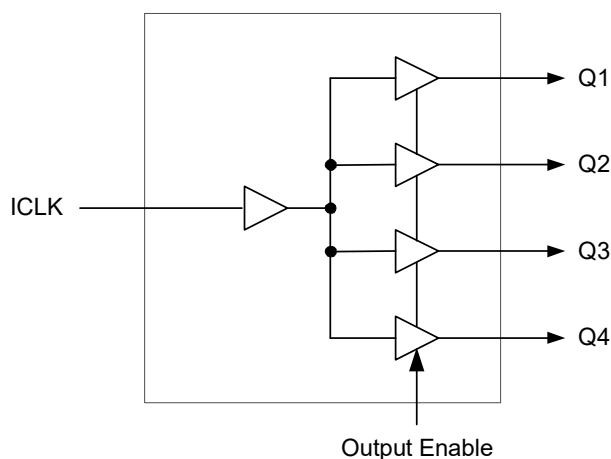


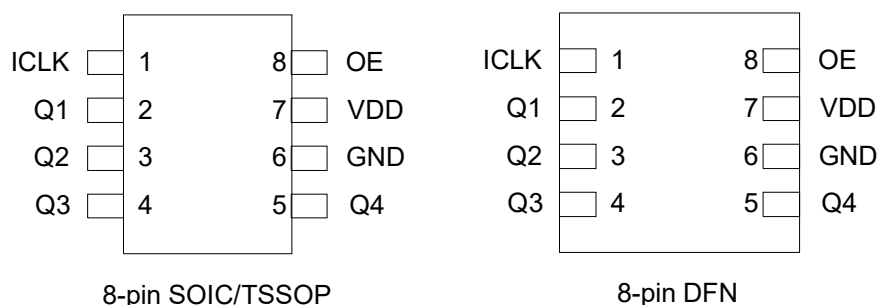
Figure 1. Block Diagram

Contents

1. Pin Information	3
1.1 Pin Assignments	3
1.2 Pin Descriptions	3
1.3 External Components	3
2. Specifications	4
2.1 Absolute Maximum Ratings	4
2.2 Recommended Operating Conditions	4
2.3 Thermal Specifications	4
2.3.1 8-SOIC	4
2.3.2 8-TSSOP	4
2.3.3 8-DFN	5
2.4 Electrical Specifications	5
2.4.1 DC Electrical Characteristics	5
2.4.2 AC Electrical Characteristics	6
2.5 Phase Noise Plots	8
2.6 Test Load and Circuit	9
3. Package Outline Drawings	9
4. Marking Diagrams	9
5. Ordering Information	10
6. Revision History	10

1. Pin Information

1.1 Pin Assignments



1.2 Pin Descriptions

Pin Number	Pin Name	Pin Type	Description
1	ICLK	Input	Clock input. Internal pull-up resistor.
2	Q1	Output	Clock output 1.
3	Q2	Output	Clock output 2.
4	Q3	Output	Clock output 3.
5	Q4	Output	Clock output 4.
6	GND	Power	Connect to ground.
7	VDD	Power	Connect +1.8V, +2.5V or +3.3V.
8	OE	Input	Output Enable. Tri-states outputs when low. Internal pull-up resistor.

1.3 External Components

A minimum number of external components are required for proper operation. A decoupling capacitor of 0.01μF should be connected between VDD on pin 7 and GND on pin 6, as close to the device as possible. A 33Ω series terminating resistor may be used on each clock output if the trace is longer than 1 inch.

2. Specifications

2.1 Absolute Maximum Ratings

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions can adversely impact product reliability and result in failures not covered by warranty.

Parameter	Rating
Supply Voltage, VDD	3.465V
All Inputs and Outputs	-0.5 V to 3.465V
Ambient Operating Temperature, Extended	-40 to +105°C
Storage Temperature	-65 to +150°C
Junction Temperature	125°C
Soldering Temperature	260°C

2.2 Recommended Operating Conditions

Parameter	Minimum	Maximum	Unit
Ambient Operating Temperature, extended	-40	+105	°C
Power Supply Voltage (measured in respect to GND)	+1.71	+3.465	V

2.3 Thermal Specifications

2.3.1 8-SOIC

Parameter	Symbol	Conditions	Typical	Unit
Thermal Resistance Junction to Ambient	Θ_{JA}	Still air	150	°C/W
		1m/s air flow	140	
		3m/s air flow	120	
Thermal Resistance Junction to Board	Θ_{JB}		89	
Thermal Resistance Junction to Case	Θ_{JC}		40	

2.3.2 8-TSSOP

Parameter	Symbol	Conditions	Typical	Unit
Thermal Resistance Junction to Ambient	Θ_{JA}	Still air	149.1	°C/W
		1m/s air flow	143.3	
		2m/s air flow	137.9	
		3m/s air flow	133.8	
Thermal Resistance Junction to Board	Θ_{JB}		153	
Thermal Resistance Junction to Case	Θ_{JC}		64.2	

2.3.3 8-DFN

Parameter	Symbol	Conditions	Typical	Unit
Thermal Resistance Junction to Ambient	Θ_{JA}	Still air	140.7	°C/W
		1m/s air flow	136.5	
		2m/s air flow	133.3	
		3m/s air flow	131.4	
Thermal Resistance Junction to Board	Θ_{JB}		93.8	
Thermal Resistance Junction to Case	Θ_{JC}		64.5	

2.4 Electrical Specifications

2.4.1 DC Electrical Characteristics

VDD = 1.8V ±5%, Ambient temperature -40° to +105°C, unless stated otherwise

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Operating Voltage	VDD		1.71	-	1.89	V
Input High Voltage, ICLK	V _{IH}	[1]	0.7xVDD	-	1.89	V
Input Low Voltage, ICLK	V _{IL}	[1]	-	-	0.3xVDD	V
Input High Voltage, OE	V _{IH}		0.7xVDD	-	VDD	V
Input Low Voltage, OE	V _{IL}		-	-	0.3xVDD	V
Output High Voltage	V _{OH}	I _{OH} = -10mA	1.3	-	-	V
Output Low Voltage	V _{OL}	I _{OL} = 10mA	-	-	0.35	V
Operating Supply Current	IDD	No load, 135MHz	-	13	-	mA
Nominal Output Impedance	Z _O		-	17	-	Ω
Input Capacitance	C _{IN}	OE pin	-	5	-	pF

1. Nominal switching threshold is VDD/2.

VDD = 2.5V ±5%, Ambient temperature -40° to +105°C, unless stated otherwise

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Operating Voltage	VDD		2.375	-	2.625	V
Input High Voltage, ICLK	V _{IH}	[1]	0.7xVDD	-	2.625	V
Input Low Voltage, ICLK	V _{IL}	[1]	-	-	0.3xVDD	V
Input High Voltage, OE	V _{IH}		0.7xVDD	-	VDD	V
Input Low Voltage, OE	V _{IL}		-	-	0.3xVDD	V
Output High Voltage	V _{OH}	I _{OH} = -16mA	1.8	-	-	V
Output Low Voltage	V _{OL}	I _{OL} = 16mA	-	-	0.5	V
Operating Supply Current	IDD	No load, 135MHz	-	18	-	mA
Nominal Output Impedance	Z _O		-	17	-	Ω
Input Capacitance	C _{IN}	OE pin	-	5	-	pF

1. Nominal switching threshold is VDD/2.

VDD = 3.3V ±5%, Ambient temperature -40° to +105°C, unless stated otherwise

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Operating Voltage	VDD		3.135	-	3.465	V
Input High Voltage, ICLK	V _{IH}	[1]	0.7xVDD	-	3.465	V
Input Low Voltage, ICLK	V _{IL}	[1]	-	-	0.3xVDD	V
Input High Voltage, OE	V _{IH}		0.7xVDD	-	VDD	V
Input Low Voltage, OE	V _{IL}		-	-	0.3xVDD	V
Output High Voltage	V _{OH}	I _{OH} = -25mA	2.2	-	-	V
Output Low Voltage	V _{OL}	I _{OL} = 25mA	-	-	0.7	V
Operating Supply Current	IDD	No load, 135MHz	-	22	-	mA
Nominal Output Impedance	Z _O		-	17	-	Ω
Input Capacitance	C _{IN}	OE pin	-	5	-	pF

1. Nominal switching threshold is VDD/2.

2.4.2 AC Electrical Characteristics

VDD = 1.8V ±5%, Ambient temperature -40° to +105°C, unless stated otherwise

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Output Frequency		5pF load [1]	-	-	200	MHz
Output Clock Rise Time	t _{OR}	0.36 to 1.44V	-	0.6	1.0	ns
Output Clock Fall Time	t _{OF}	1.44 to 0.36V	-	0.6	1.0	ns
Propagation Delay		135MHz [2]	1.5	2	4	ns
Buffer Additive Phase Jitter, RMS		125MHz, Integration range: 12kHz–20MHz	-	0.03	0.05	ps
Output to Output Skew		Rising edges at VDD/2 [3]	-	50	65	ps
Start-up Time	t _{START-UP}	Part start-up time for valid outputs after VDD ramp-up	-	-	2	ms
Output Enable Time	t _{EN}	CL ≤ 5pF	-	-	3	cycles
Output Disable Time	t _{DIS}	CL ≤ 5pF	-	-	3	cycles

1. With external series resistor of 33Ω positioned close to each output pin.
2. With rail to rail input clock.
3. Between any 2 outputs with equal loading.

VDD = 2.5V ±5%, Ambient temperature -40° to +105°C, unless stated otherwise

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Output Frequency		5pF load [1]	-	-	200	MHz
Output Clock Rise Time	t _{OR}	0.5 to 2.0V	-	0.6	1.0	ns
Output Clock Fall Time	t _{OF}	2.0 to 0.5V	-	0.6	1.0	ns
Propagation Delay		135MHz [2]	1.8	2.5	4.5	ns
Buffer Additive Phase Jitter, RMS		125MHz, Integration range: 12kHz–20MHz	-	0.035	0.05	ps
Output to Output Skew		Rising edges at VDD/2 [3]	-	50	65	ps
Start-up Time	t _{START-UP}	Part start-up time for valid outputs after VDD ramp-up	-	-	2	ms
Output Enable Time	t _{EN}	CL ≤ 5pF	-	-	3	cycles
Output Disable Time	t _{DIS}	CL ≤ 5pF	-	-	3	cycles

1. With external series resistor of 33Ω positioned close to each output pin.
2. With rail to rail input clock.
3. Between any 2 outputs with equal loading.

VDD = 3.3V ±5%, Ambient temperature -40° to +105°C, unless stated otherwise

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Output Frequency		5pF load [1]	-	-	200	MHz
Output Clock Rise Time	t _{OR}	0.66 to 2.64V	-	0.6	1.0	ns
Output Clock Fall Time	t _{OF}	2.64 to 0.66V	-	0.6	1.0	ns
Propagation Delay		135MHz [2]	1.5	2	4	ns
Buffer Additive Phase Jitter, RMS		125MHz, Integration range: 12kHz–20MHz	-	0.037	0.05	ps
Output to Output Skew		Rising edges at VDD/2 [3]	-	50	65	ps
Start-up Time	t _{START-UP}	Part start-up time for valid outputs after VDD ramp-up	-	-	2	ms
Output Enable Time	t _{EN}	CL ≤ 5pF	-	-	3	cycles
Output Disable Time	t _{DIS}	CL ≤ 5pF	-	-	3	cycles

1. With external series resistor of 33Ω positioned close to each output pin.
2. With rail to rail input clock.
3. Between any 2 outputs with equal loading.

2.5 Phase Noise Plots

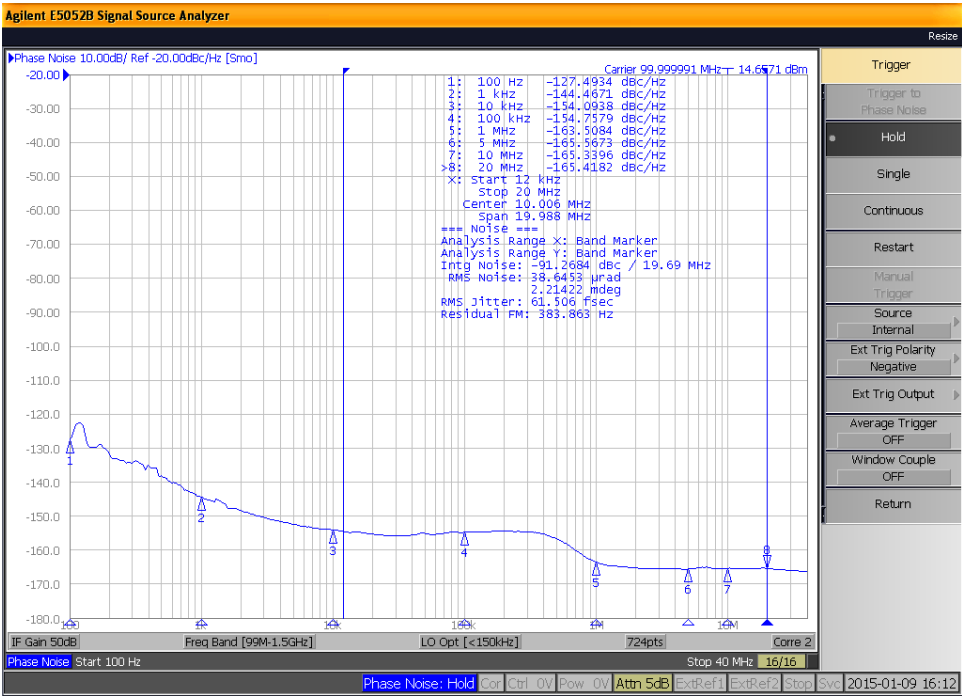


Figure 2. 551S Reference Phase Noise 62fs (12kHz to 20MHz)

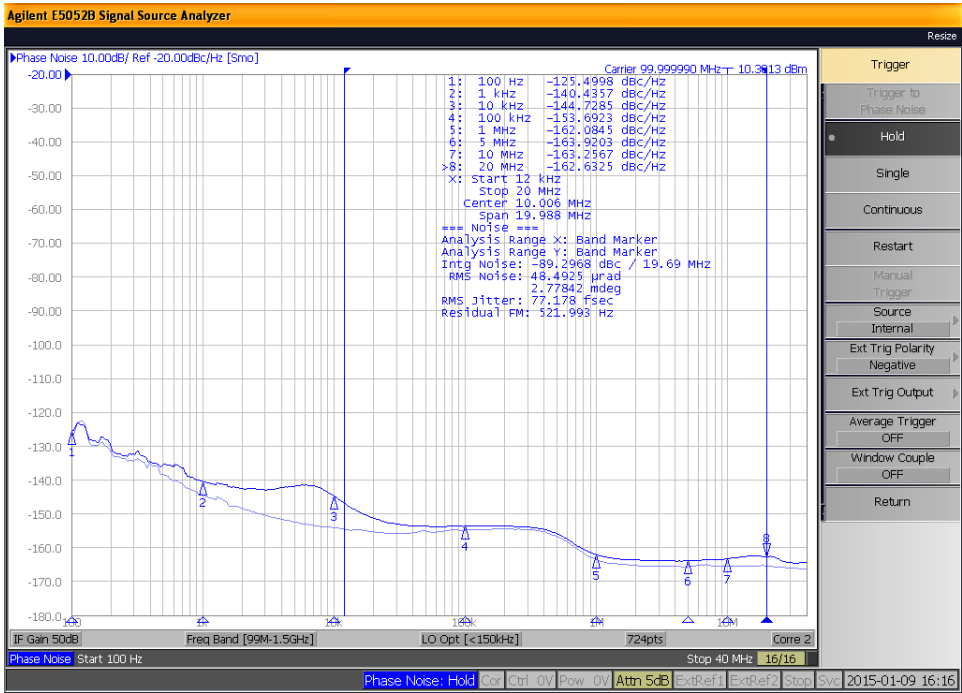
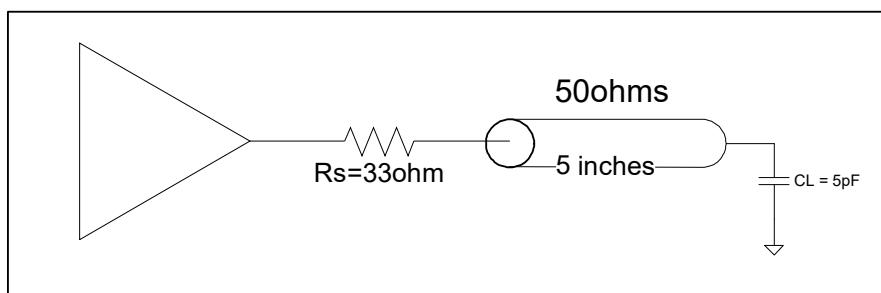


Figure 3. 551S Output Phase Noise 77fs (12kHz to 20MHz)

The phase noise plots above show the low Additive Jitter of the 551S high-performance buffer. With an integration range of 12kHz to 20MHz, the reference input has about 62fs of RMS phase jitter while the output has about 77fs of RMS phase jitter. This results in a low Additive Phase Jitter of only 45fs.

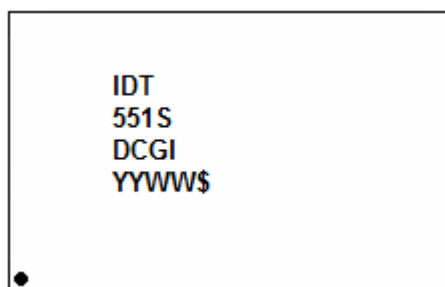
2.6 Test Load and Circuit



3. Package Outline Drawings

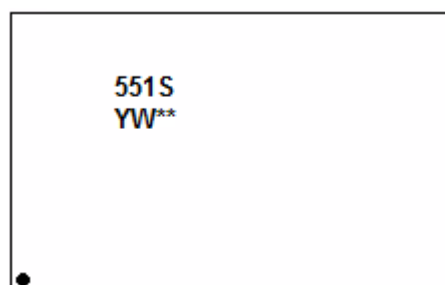
The package outline drawings are located at the end of this document and are accessible from the Renesas website (see [Ordering Information](#) for package links). The package information is the most current data available and is subject to change without revision of this document.

4. Marking Diagrams



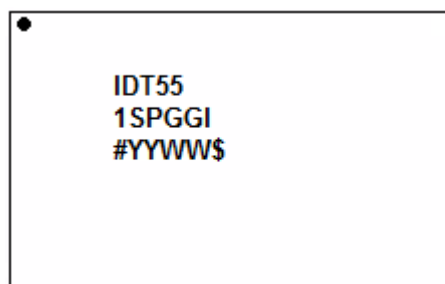
8-SOIC

- Lines 1, 2, and 3: part number.
- Line 4:
 - “YYWW” are the last digits of the year and week that the part was assembled.
 - “\$” denotes the mark code.



8-DFN

- Line 1: truncated part number.
- Line 2:
 - “YW” are the last digit of the year and week that the part was assembled.
 - “**” denotes the lot sequence.



8-TSSOP

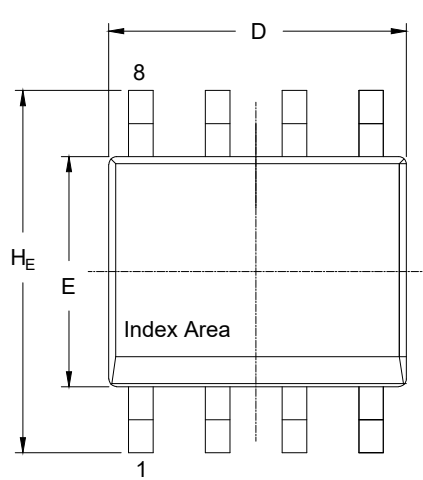
- Lines 1 and 2: part number.
- Line 3:
 - “#” denotes the stepping number.
 - “YYWW” are the last digits of the year and week that the part was assembled.
 - “\$” denotes the mark code.

5. Ordering Information

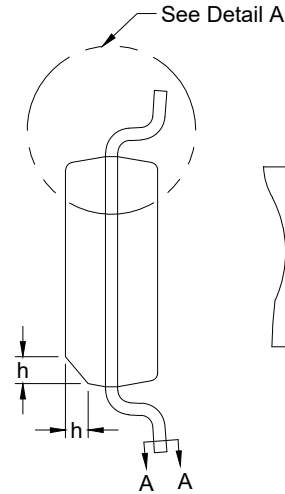
Part Number	Package	Carrier Type	Temperature
551SDCGI	8-SOIC, 0.150" body	Tubes	-40°C to +105°C
551SDCGI8		Tape and Reel	
551SCMGI	8-DFN, 2.0 × 2.0 × 0.5 mm	Cut Tape	
551SCMGI8		Tape and Reel	
551SPGGI	8-TSSOP, 4.4 × 3.0 mm	Tubes	
551SPGGI8		Tape and Reel	

6. Revision History

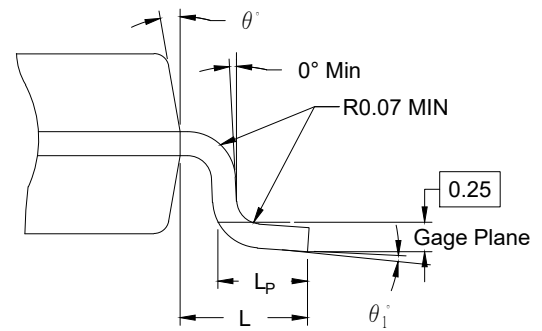
Revision	Date	Description
2.03	Jul 4, 2025	Added 8-TSSOP and 8-DFN thermal specifications.
2.02	Dec 13, 2023	Updated POD link for 8-DFN to CMG8D1.
2.01	Dec 21, 2022	- Updated Output Clock Rise/Fall Time in 2.5V and 3.3V AC Electrical Characteristics tables. - Removed footnote 4 in 1.8V, 2.5V and 3.3V AC Electrical Characteristics tables.
2.00	May 21, 2021	Updated 3.3V AC Electrical Characteristics table (Parameter, Symbol, Test Conditions).
1.30	Mar 12, 2021	- Added 8-TSSOP package information. - Reformatted datasheet to latest template.
1.20	Sep 20, 2018	- Added Thermal Resistance Junction to Board to Thermal Characteristics table. - Updated Package Outline Drawings section.
1.00	Mar 18, 2015	Initial release.



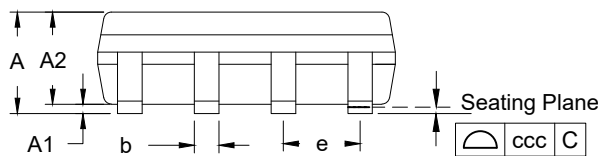
Top View



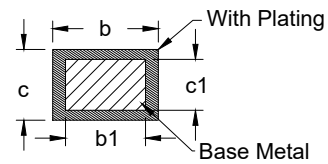
Side View



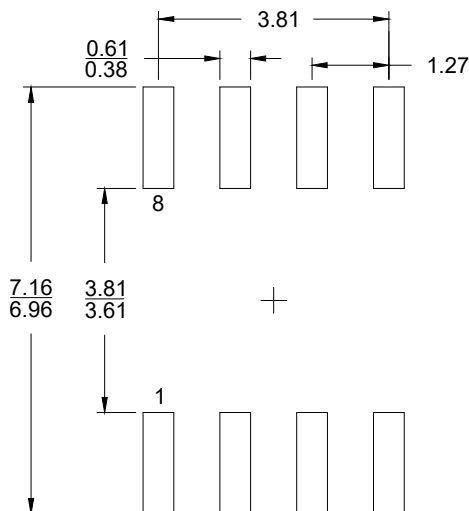
Detail A
(Rotated 90° CW)



Side View



Section A-A



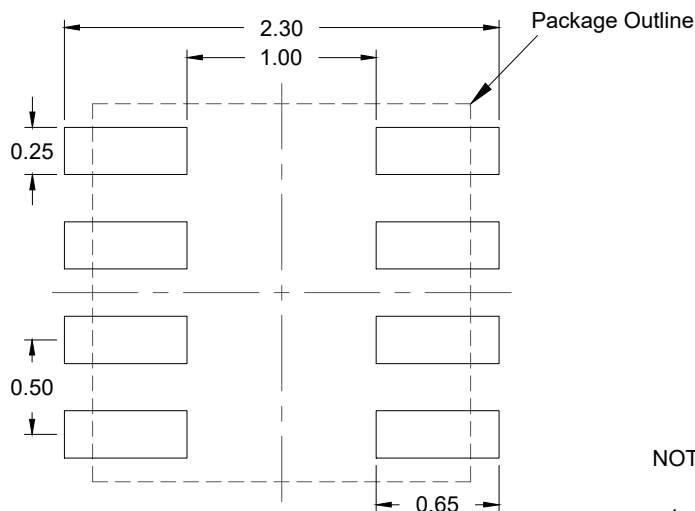
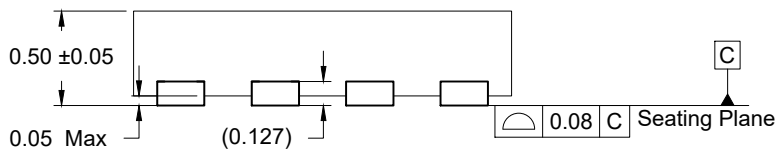
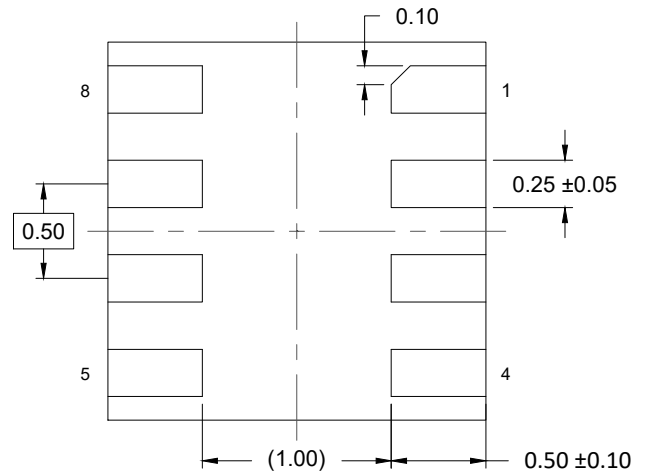
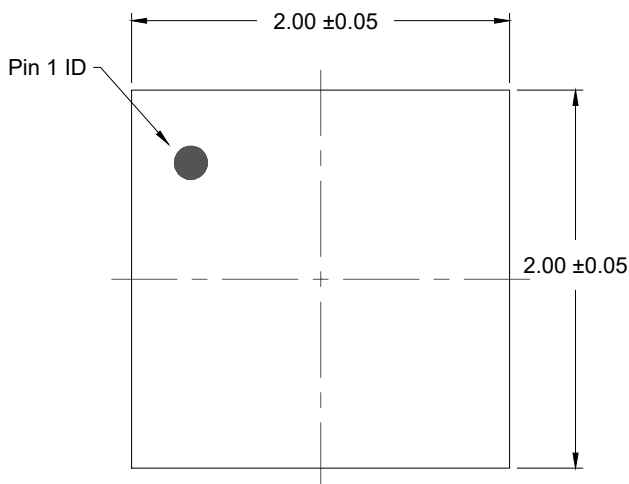
RECOMMENDED LAND PATTERN
(PCB Top View, SMD Design)

SYMBOLS	MIN.	NOM.	MAX.
A	—	—	1.75
A1	0.10	—	0.25
A2	1.25	—	—
b	0.31	—	0.51
D	4.80	4.90	5.00
H _E	5.80	6.00	6.20
E	3.80	3.90	4.00
e	1.27 BSC		
ccc	0.10		
L _P	0.40	—	1.27
L	(1.00)		
θ°	5°	—	15°
θ ₁ °	0°	—	8°
h	0.25	—	0.50
b	0.31	—	0.51
b1	0.28	—	0.48
c	0.10	—	0.25
c1	0.10	—	0.25

UNIT : MM

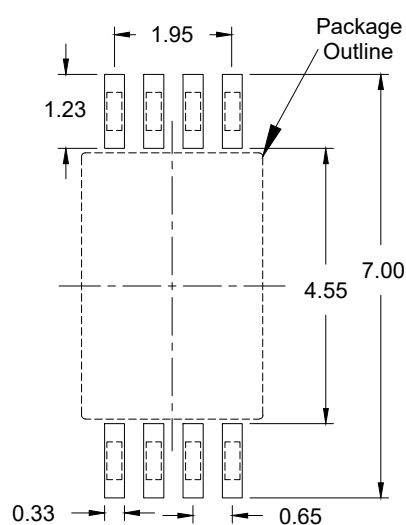
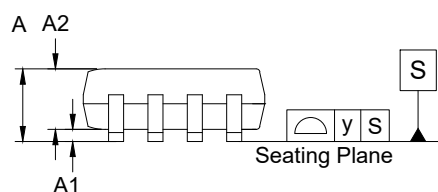
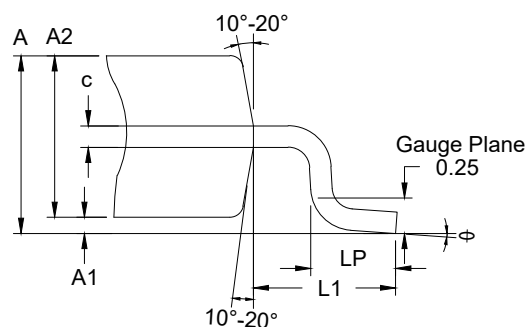
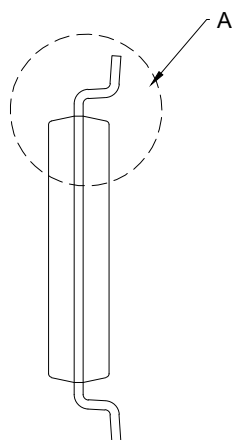
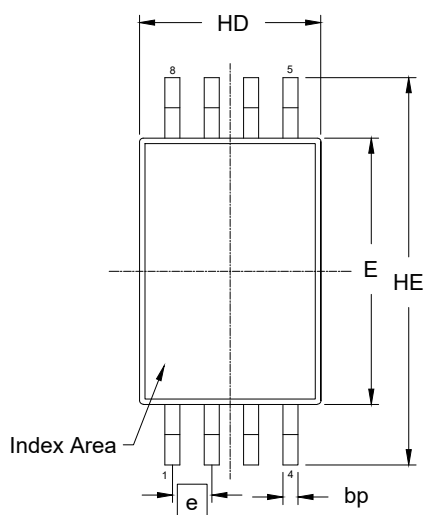
NOTES:

1. JEDEC compatible.
2. All dimensions are in mm and angles are in degrees.
3. Use ±0.05 mm for the non-toleranced dimensions.
4. Foot length is measured at gauge plane 0.25 mm above seating plane.



NOTES:

1. JEDEC compatible.
2. All dimensions are in mm and angles are in degrees.
3. Use ± 0.05 mm for the non-toleranced dimensions.
4. Numbers in () are for references only.



Reference Symbol	Dimension in mm		
	Min	Nom	Max
E	4.30	4.40	4.50
A2	0.80	-	1.05
HD	2.90	3.00	3.10
HE	6.20	6.40	6.60
A	0.85	-	1.20
A1	0.05	0.10	0.15
bp	0.19	0.25	0.30
c	0.09	-	0.20
θ	0.00	-	8.00
e	0.65 BSC		
y	-	-	0.10
LP	0.50	0.625	0.75
L1	-	1.00	-

NOTES:

1. JEDEC compatible.
2. All dimensions are in mm and angles are in degrees.
3. Use ± 0.05 mm for the non-toleranced dimensions.
4. Foot length is measured at gauge plane 0.25 mm above seating plane.

IMPORTANT NOTICE AND DISCLAIMER

RENESAS ELECTRONICS CORPORATION AND ITS SUBSIDIARIES ("RENESAS") PROVIDES TECHNICAL SPECIFICATIONS AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES "AS IS" AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS OR IMPLIED, INCLUDING, WITHOUT LIMITATION, ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE, OR NON-INFRINGEMENT OF THIRD-PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for developers who are designing with Renesas products. You are solely responsible for (1) selecting the appropriate products for your application, (2) designing, validating, and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, or other requirements. These resources are subject to change without notice. Renesas grants you permission to use these resources only to develop an application that uses Renesas products. Other reproduction or use of these resources is strictly prohibited. No license is granted to any other Renesas intellectual property or to any third-party intellectual property. Renesas disclaims responsibility for, and you will fully indemnify Renesas and its representatives against, any claims, damages, costs, losses, or liabilities arising from your use of these resources. Renesas' products are provided only subject to Renesas' Terms and Conditions of Sale or other applicable terms agreed to in writing. No use of any Renesas resources expands or otherwise alters any applicable warranties or warranty disclaimers for these products.

(Disclaimer Rev.1.01)

Corporate Headquarters

TOYOSU FORESIA, 3-2-24 Toyosu,
Koto-ku, Tokyo 135-0061, Japan
www.renesas.com

Contact Information

For further information on a product, technology, the most up-to-date version of a document, or your nearest sales office, please visit www.renesas.com/contact-us/.

Trademarks

Renesas and the Renesas logo are trademarks of Renesas Electronics Corporation. All trademarks and registered trademarks are the property of their respective owners.