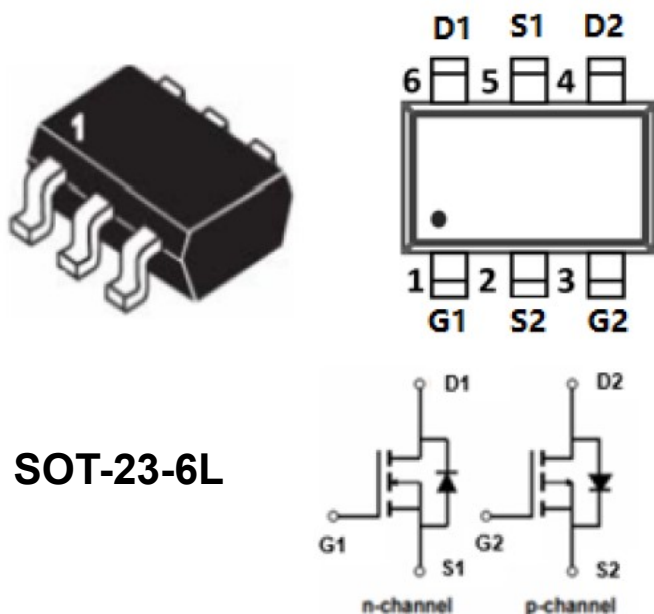




N-Channel and P-Channel Complementary Power MOSFET

Product Summary



SOT-23-6L

NMOS

- V_{DS} 20V
- I_D 5.6A
- $R_{DS(ON)}$ (at $V_{GS}=4.5V$) <25mohm
- $R_{DS(ON)}$ (at $V_{GS}=2.5V$) <32mohm
- $R_{DS(ON)}$ (at $V_{GS}=1.8V$) <49mohm

PMOS

- V_{DS} -20V
- I_D -3.7A
- $R_{DS(ON)}$ (at $V_{GS}=-4.5V$) <64mohm
- $R_{DS(ON)}$ (at $V_{GS}=-2.5V$) <80mohm
- $R_{DS(ON)}$ (at $V_{GS}=-1.8V$) <110mohm

- 100% ∇V_{DS} Tested

General Description

- Trench Power LV MOSFET technology
- High density cell design for low $R_{DS(ON)}$
- High Speed switching

Applications

- Wireless charger
- Load switch
- Power management

■ Absolute Maximum Ratings ($T_A=25^\circ\text{C}$ unless otherwise noted)

Parameter		Symbol	N-Channel	P-Channel	Unit
Drain-source Voltage		V_{DS}	20	-20	V
Gate-source Voltage		V_{GS}	± 10	± 10	V
Drain Current	$T_A=25^\circ\text{C}$	I_D	5.6	-3.7	A
	$T_A=70^\circ\text{C}$		4.5	-3	
Pulsed Drain Current ^A		I_{DM}	19	-15	A
Total Power Dissipation	$T_A=25^\circ\text{C}$	P_D	1.3	1.3	W
	$T_A=70^\circ\text{C}$		0.8	0.8	W
Thermal Resistance Junction-to-Ambient ^B		$R_{\theta JA}$	96	96	$^\circ\text{C}/\text{W}$
Junction and Storage Temperature Range		T_J, T_{STG}	-55~+150	-55~+150	$^\circ\text{C}$

■ Ordering Information (Example)

PREFERRED P/N	PACKING CODE	Marking	MINIMUM PACKAGE(pcs)	INNER BOX QUANTITY(pcs)	OUTER CARTON QUANTITY(pcs)	DELIVERY MODE
YJS2308A	F2	2308	3000	30000	120000	7" reel



YJS2308A

■ N-MOS Electrical Characteristics ($T_J=25^{\circ}\text{C}$ unless otherwise noted)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Static Parameter						
Drain-Source Breakdown Voltage	BV _{DSS}	V _{GS} =0V, I _D =250μA	20			V
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} =20V, V _{GS} =0V			1	μA
Gate-Body Leakage Current	I _{GSS}	V _{GS} =±10V, V _{DS} =0V			±100	nA
Gate Threshold Voltage	V _{GS(th)}	V _{DS} = V _{GS} , I _D =250μA	0.5	0.62	1.0	V
Static Drain-Source On-Resistance	R _{DS(ON)}	V _{GS} =4.5V, I _D =4.5A		19.5	25	mΩ
		V _{GS} =2.5V, I _D =3A		25	32	
		V _{GS} =1.8V, I _D =2A		33	49	
Diode Forward Voltage	V _{SD}	I _S =5.6A, V _{GS} =0V			1.2	V
Dynamic Parameters						
Input Capacitance	C _{iss}	V _{DS} =10V, V _{GS} =0V, f=1MHZ		418		pF
Output Capacitance	C _{oss}			82		
Reverse Transfer Capacitance	C _{rss}			70		
Switching Parameters						
Total Gate Charge	Q _g	V _{GS} =4.5V, V _{DS} =10V, I _D =4.5A		6.05		nC
Gate-Source Charge	Q _{gs}			1.07		
Gate-Drain Charge	Q _{gd}			1.95		
Reverse Recovery Chrage	Q _{rr}	I _F =4.5A, di/dt=100A/us		1.38		
Reverse Recovery Time	t _{rr}			17.9		
Turn-on Delay Time	t _{D(on)}	V _{GS} =4.5V, V _{DS} =10V, R _L =1Ω R _{GEN} =3Ω		4.2		ns
Turn-on Rise Time	t _r			19.8		
Turn-off Delay Time	t _{D(off)}			22.6		
Turn-off fall Time	t _f			23.2		

A. Pulse Test: Pulse Width $\leq 300\mu s$, Duty cycle $\leq 2\%$.

B. $R_{\theta JA}$ is the sum of the junction-to-case and case-to-ambient thermal resistance, where the case thermal reference is defined as the solder mounting surface of the drain pins. $R_{\theta JC}$ is guaranteed by design, while $R_{\theta JA}$ is determined by the board design. The maximum rating presented here is based on mounting on a 1 in 2 pad of 2oz copper.



YJS2308A

■ P-MOS Electrical Characteristics ($T_J=25^{\circ}\text{C}$ unless otherwise noted)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Static Parameter						
Drain-Source Breakdown Voltage	BV _{DSS}	V _{GS} =0V, I _D =-250μA	-20			V
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} =-20V, V _{GS} =0V			-1	μA
Gate-Body Leakage Current	I _{GSS}	V _{GS} =± 10V, V _{DS} =0V			± 100	nA
Gate Threshold Voltage	V _{GS(th)}	V _{DS} = V _{GS} , I _D =-250μA	-0.4	-0.62	-1.0	V
Static Drain-Source On-Resistance	R _{DS(ON)}	V _{GS} =-4.5V, I _D =-3.5A		49	64	mΩ
		V _{GS} =-2.5V, I _D =-3A		59	80	
		V _{GS} =-1.8V, I _D =-2A		79	110	
Diode Forward Voltage	V _{SD}	I _S =-3.7A, V _{GS} =0V			-1.2	V
Dynamic Parameters						
Input Capacitance	C _{iss}	V _{DS} =-10V, V _{GS} =0V, f=1MHZ		438		pF
Output Capacitance	C _{oss}			76		
Reverse Transfer Capacitance	C _{rss}			62		
Switching Parameters						
Total Gate Charge	Q _g	V _{GS} =-10V, V _{DS} =-15V, I _D =-3.4A		5.41		nC
Gate-Source Charge	Q _{gs}			1.17		
Gate-Drain Charge	Q _{gd}			1.24		
Reverse Recovery Chrage	Q _{rr}	I _F =-3.4A, di/dt=100A/us		4		ns
Reverse Recovery Time	t _{rr}			24.5		
Turn-on Delay Time	t _{D(on)}	V _{GS} =-4.5V, V _{DS} =-10V, I _D =-1A R _{GEN} =3Ω		6.4		
Turn-on Rise Time	t _r			21.8		
Turn-off Delay Time	t _{D(off)}			37.4		
Turn-off fall Time	t _f			34		

C. Pulse Test: Pulse Width $\leq 300\mu s$, Duty cycle $\leq 2\%$.

D. $R_{\theta JA}$ is the sum of the junction-to-case and case-to-ambient thermal resistance, where the case thermal reference is defined as the solder mounting surface of the drain pins. $R_{\theta JC}$ is guaranteed by design, while $R_{\theta JA}$ is determined by the board design. The maximum rating presented here is based on mounting on a 1 in 2 pad of 2oz copper.

■ N-MOS Typical Performance Characteristics

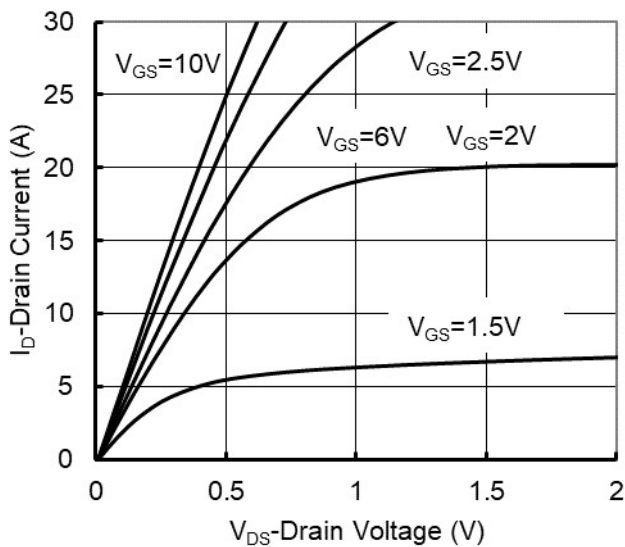


Figure1. Output Characteristics

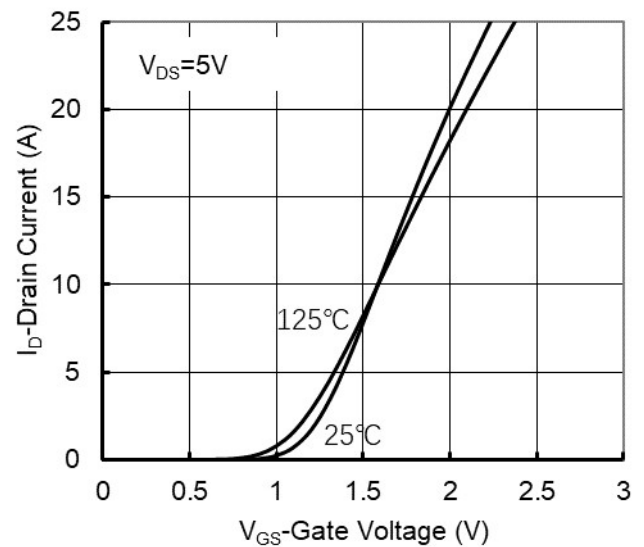


Figure2. Transfer Characteristics

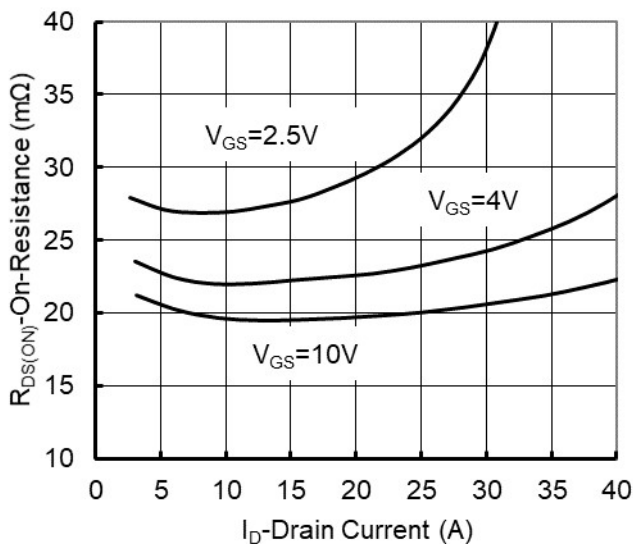


Figure 3: On-Resistance vs. Drain Current and Gate Voltage

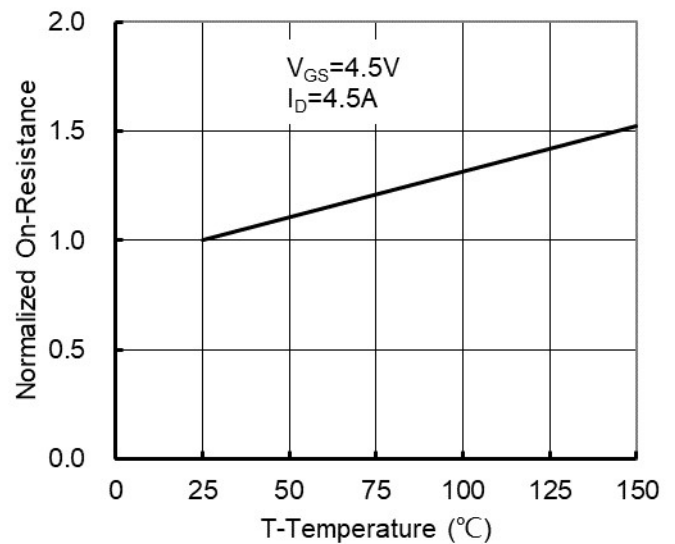


Figure 4: On-Resistance vs. Junction Temperature

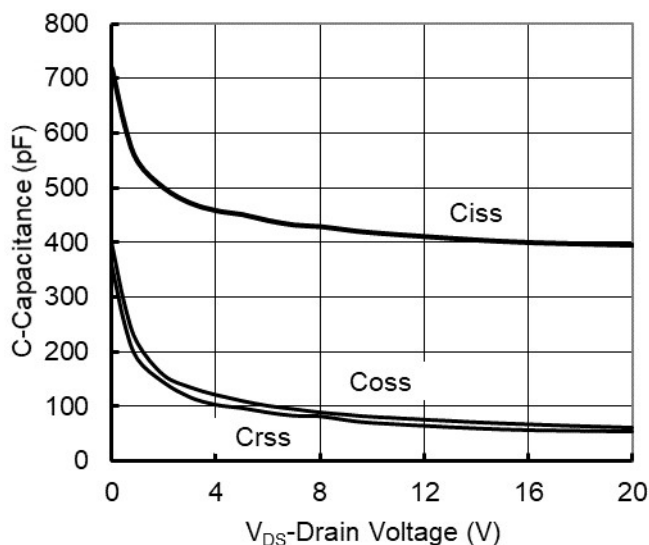


Figure5. Capacitance Characteristics

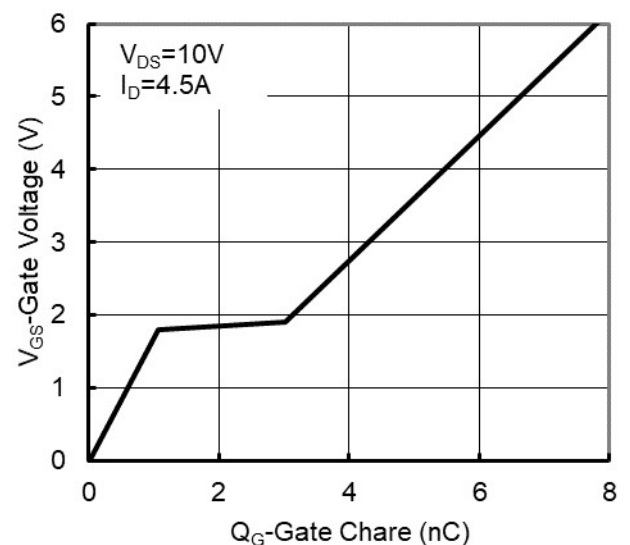


Figure6. Gate Charge

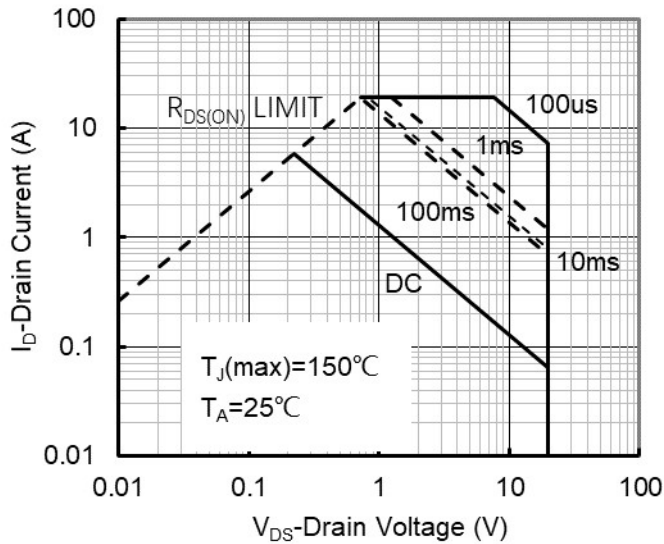


Figure7. Safe Operation Area

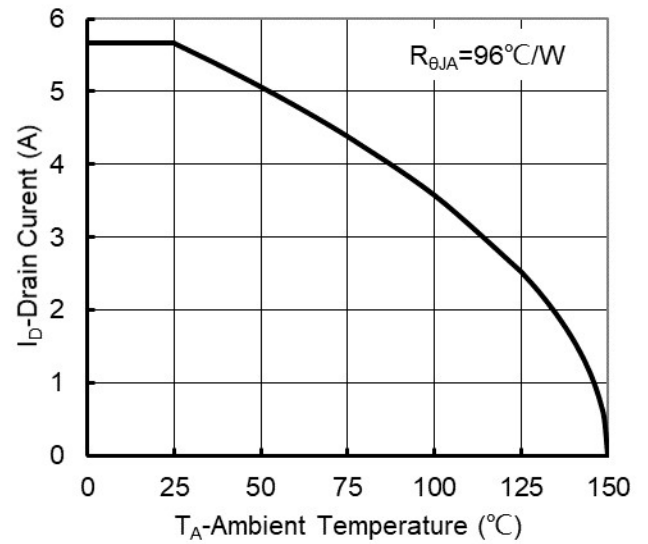


Figure8. Maximum Continuous Drain Current vs Ambient Temperature

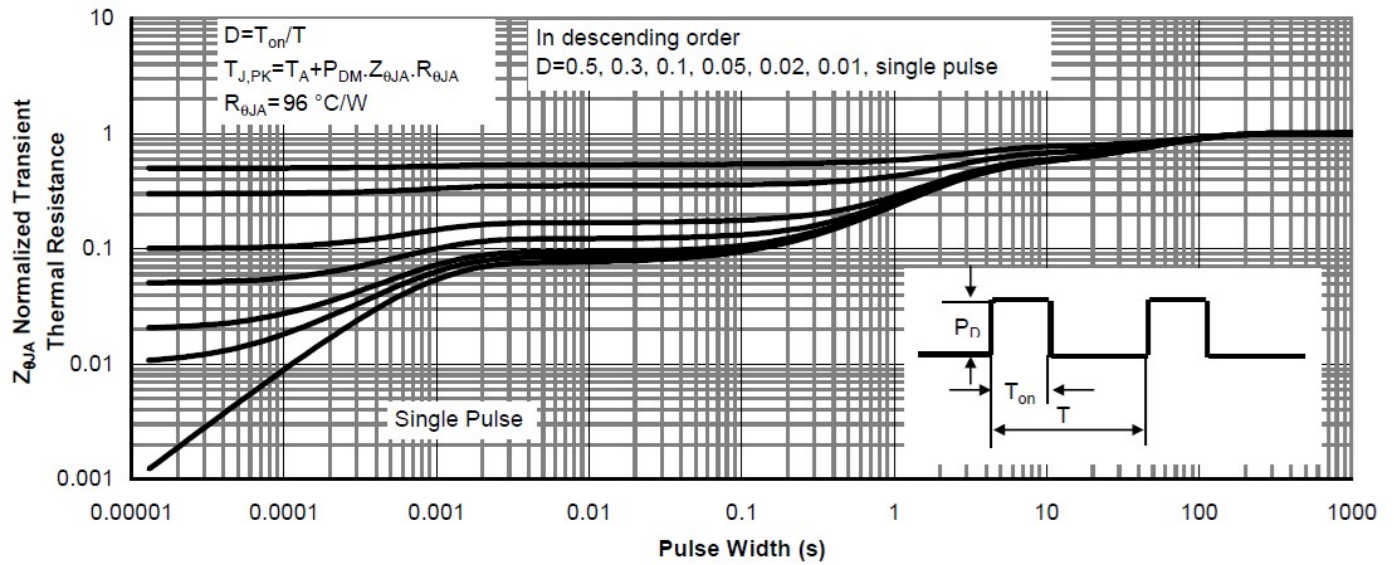


Figure9.Normalized Maximum Transient Thermal Impedance



■ P-MOS Typical Performance Characteristics

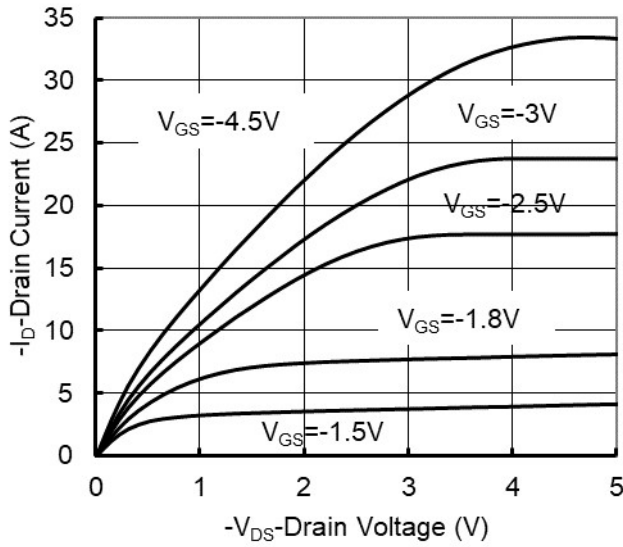


Figure1. Output Characteristics

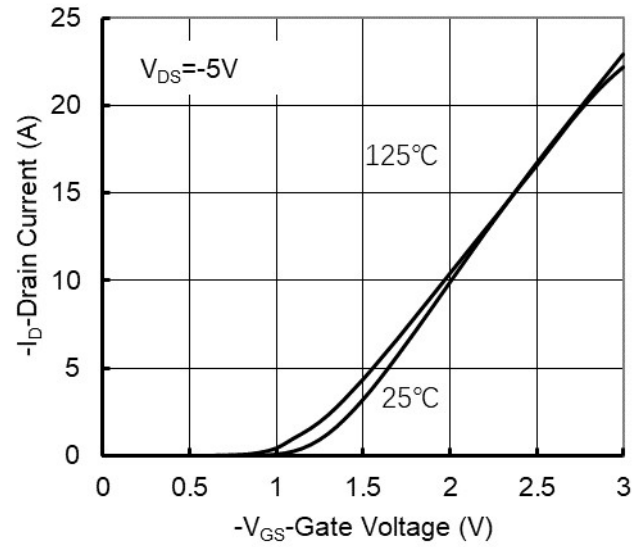


Figure2. Transfer Characteristics

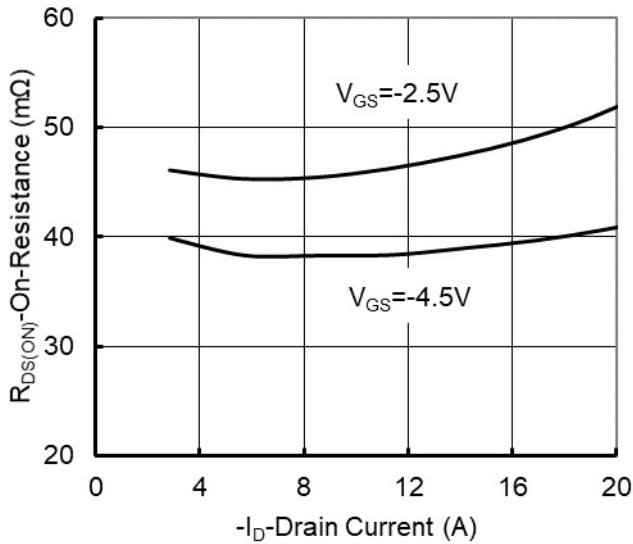


Figure 3: On-Resistance vs. Drain Current and Gate Voltage

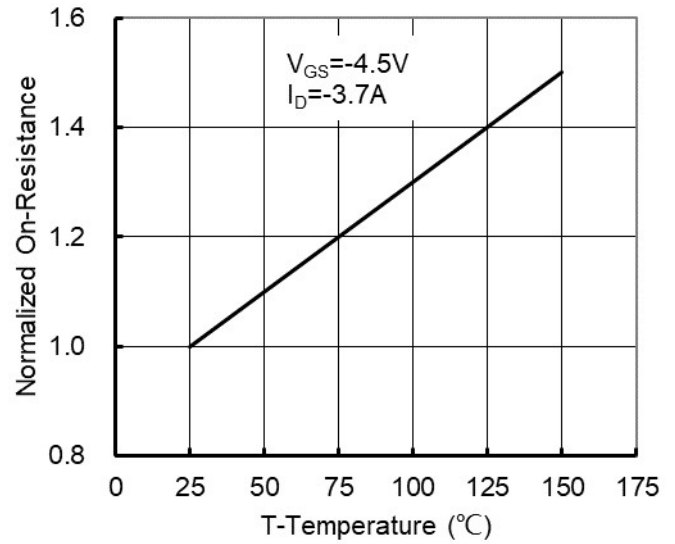


Figure 4: On-Resistance vs. Junction Temperature

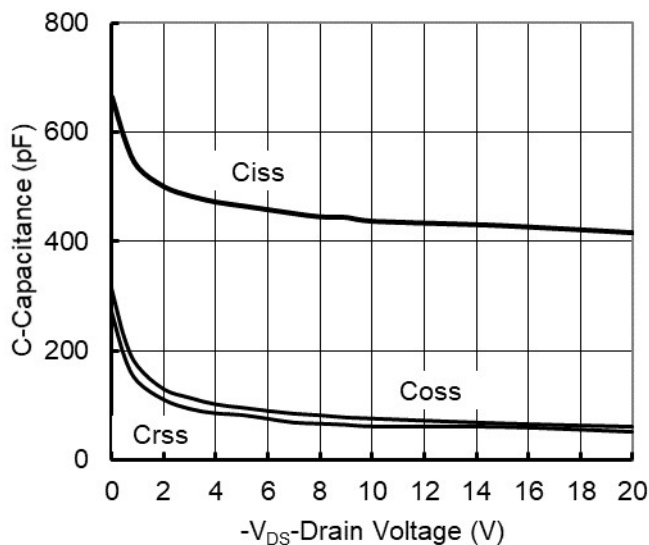


Figure5. Capacitance Characteristics

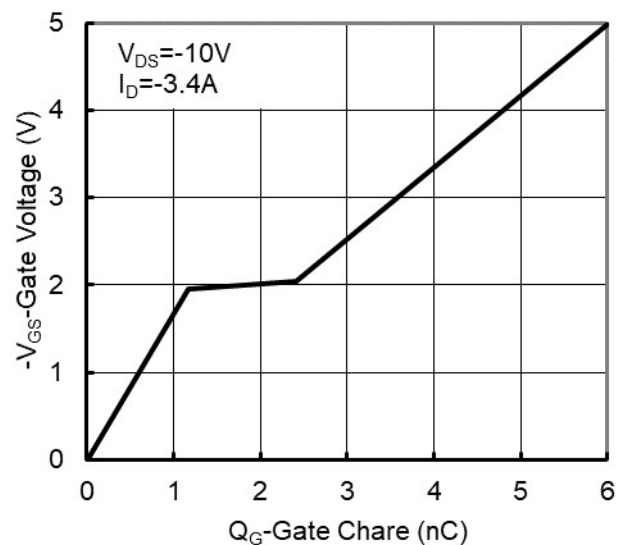


Figure6. Gate Charge

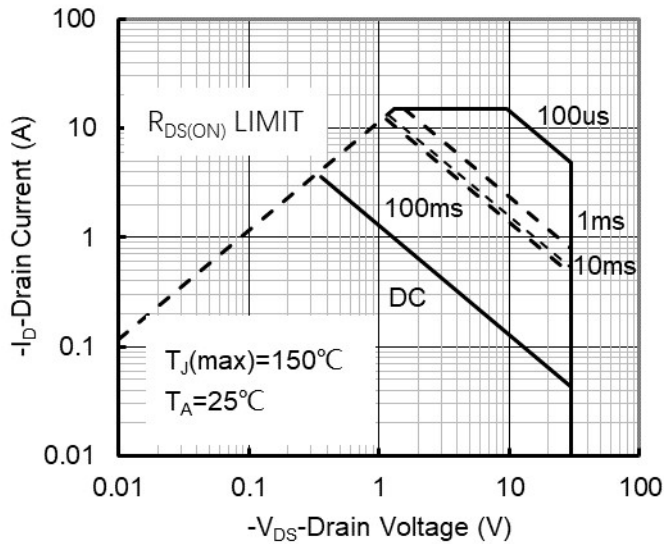


Figure7. Safe Operation Area

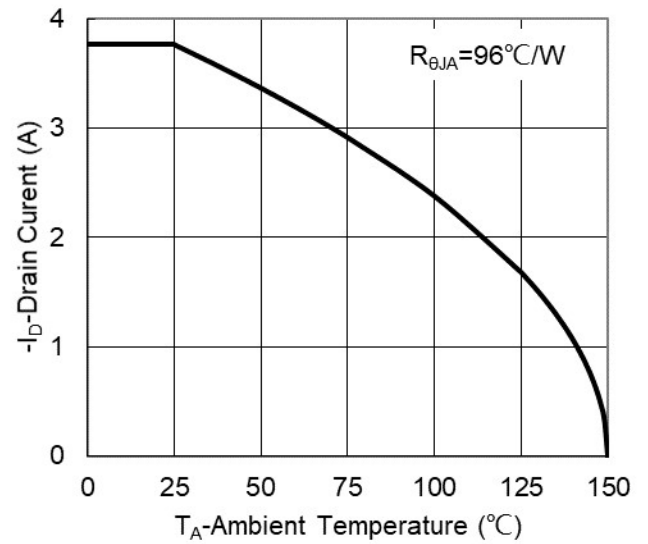


Figure8. Maximum Continuous Drain Current vs Ambient Temperature

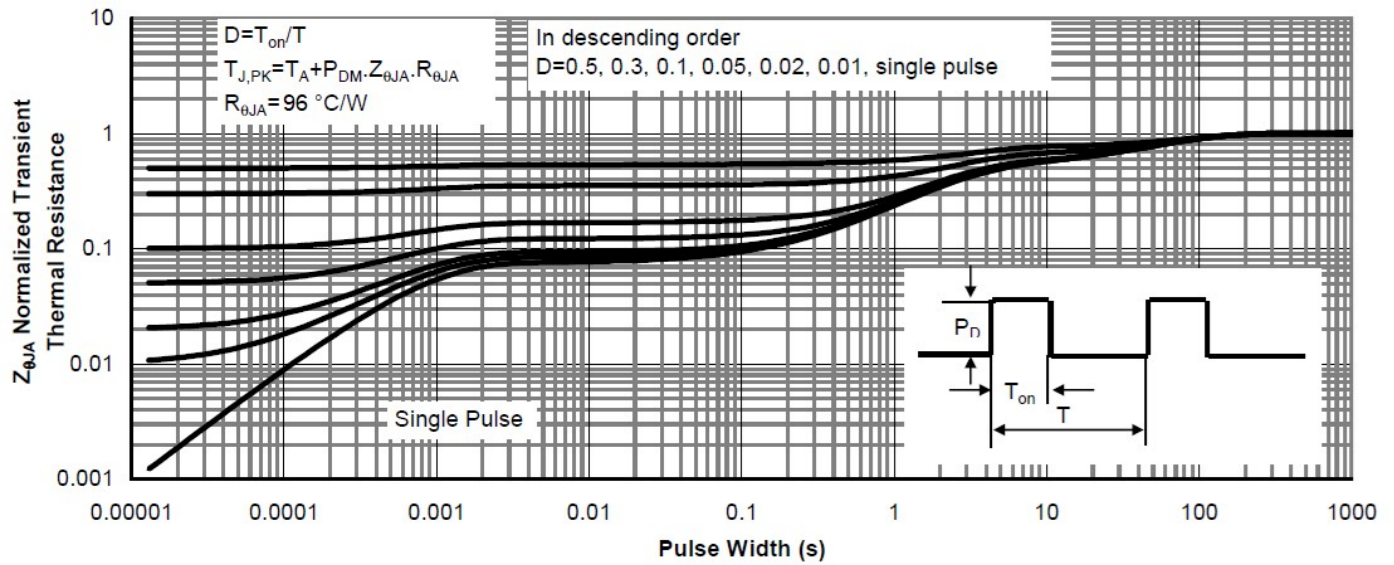
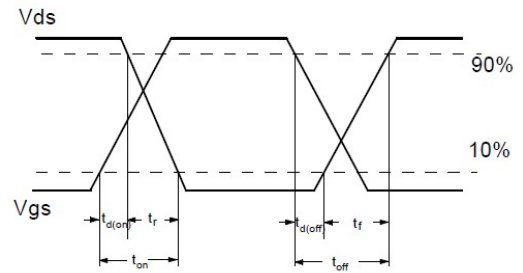
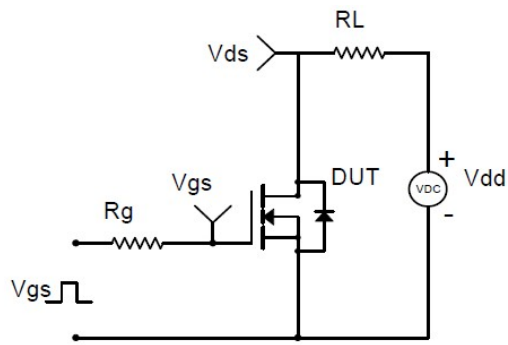
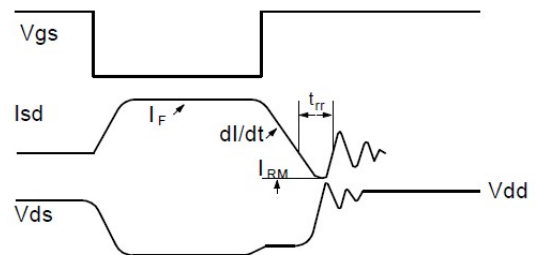
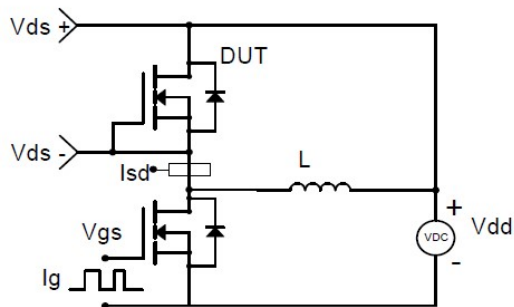


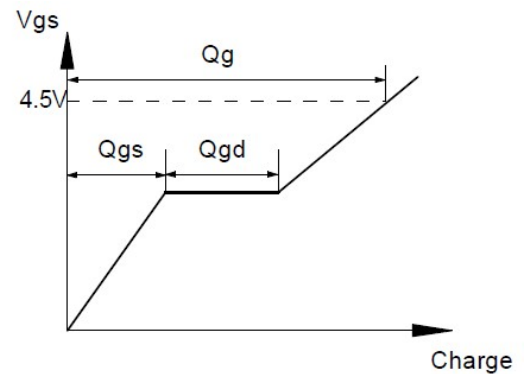
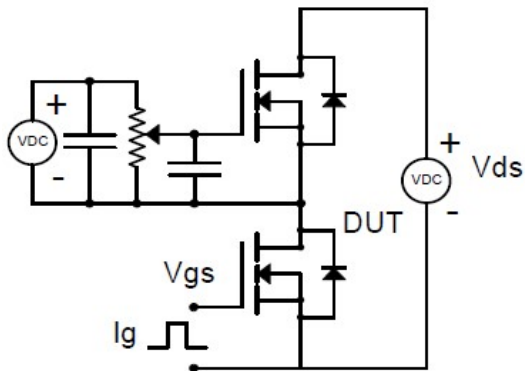
Figure9.Normalized Maximum Transient Thermal Impedance



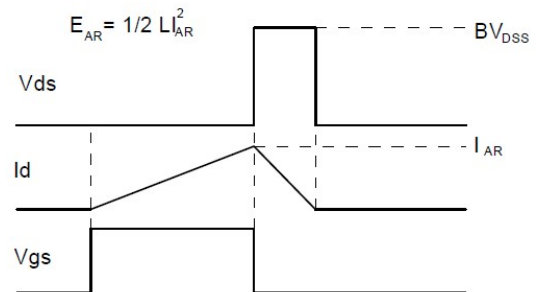
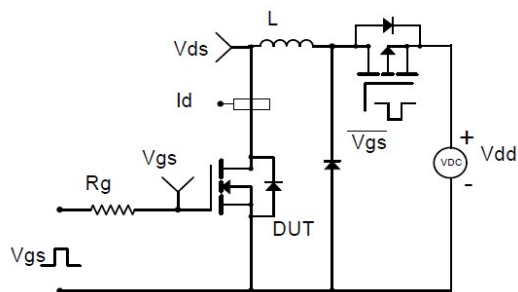
Resistive Switching Test Circuit & Waveforms



Diode Recovery Test Circuit & Waveforms



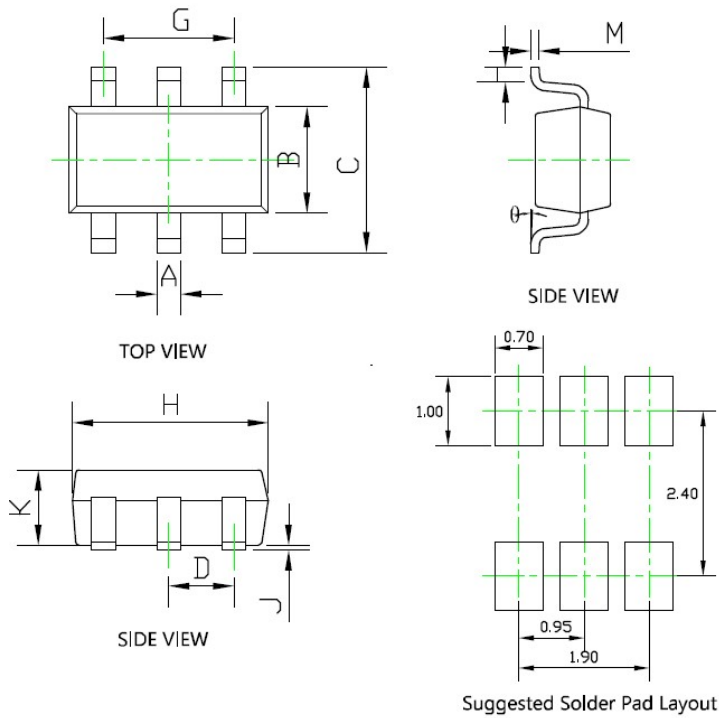
Gate Charge Test Circuit & Waveform



Unclamped Inductive Switching (UIS) Test Circuit & Waveforms



■ SOT-23-6L Package information



Note:
1,Controlling dimension:in millimeters.
2,General tolerance:±0.05mm.
3,The pad layout is for reference purposes only.

SYMBOL	DIMENSIONS			
	INCHES		Millimeter	
	MIN.	MAX.	MIN.	MAX.
A	0.012	0.020	0.300	0.500
B	0.059	0.067	1.500	1.700
C	0.104	0.116	2.650	2.950
D	0.037BSC		0.950BSC	
G	0.075BSC		1.900BSC	
H	0.111	0.119	2.820	3.020
J	0.000	0.004	0.000	0.100
K	0.041	0.045	1.050	1.150
L	0.012	0.024	0.300	0.600
M	0.004	0.008	0.100	0.200
θ	0°	8°	0°	8°



Disclaimer

The information presented in this document is for reference only. Yangzhou Yangjie Electronic Technology Co., Ltd. reserves the right to make changes without notice for the specification of the products displayed herein to improve reliability, function or design or otherwise.

The product listed herein is designed to be used with ordinary electronic equipment or devices, and not designed to be used with equipment or devices which require high level of reliability and the malfunction of which would directly endanger human life (such as medical instruments, transportation equipment, aerospace machinery, nuclear-reactor controllers, fuel controllers and other safety devices), Yangjie or anyone on its behalf, assumes no responsibility or liability for any damages resulting from such improper use of sale.

This publication supersedes & replaces all information previously supplied. For additional information, please visit our website [http:// www.21yangjie.com](http://www.21yangjie.com) , or consult your nearest Yangjie's sales office for further assistance.