

MOSFET - Power, Single N-Channel, SUPERFET® V, Easy Drive, TO247-3L 600 V, 120 mΩ, 28 A NTHL120N60S5Z

Description

SUPERFET V MOSFET Easy Drive series combines excellent switching performance without sacrificing ease of use and EMI issues for both hard and soft switching topologies.

Features

- 650 V @ $T_J = 150^\circ\text{C}$
- Typ. $R_{DS(on)} = 96\text{ m}\Omega$
- 100% Avalanche Tested
- Pb-Free, Halogen Free/BFR Free and are RoHS Compliant

Applications

- Telecom / Server Power Supplies
- EV Charger / UPS / Solar / Industrial Power Supplies

ABSOLUTE MAXIMUM RATINGS ($T_J = 25^\circ\text{C}$, Unless otherwise noted)

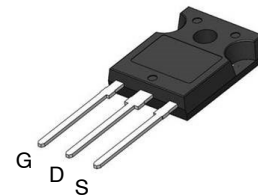
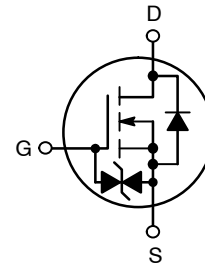
Parameter	Symbol	Value	Unit
Drain-to-Source Voltage	V_{DSS}	600	V
Gate-to-Source Voltage	DC	V_{GSS}	± 20
		AC ($f > 1\text{ Hz}$)	± 20
Continuous Drain Current	$T_C = 25^\circ\text{C}$	I_D	28*
		$T_C = 100^\circ\text{C}$	17*
Power Dissipation	$T_C = 25^\circ\text{C}$	P_D	160
Pulsed Drain Current (Note 1)	$T_C = 25^\circ\text{C}$	I_{DM}	81*
Pulsed Source Current (Body Diode) (Note 1)	$T_C = 25^\circ\text{C}$	I_{SM}	81*
Operating Junction and Storage Temperature Range	T_J, T_{STG}	-55 to +150	$^\circ\text{C}$
Source Current (Body Diode)	I_S	28*	A
Single Pulse Avalanche Energy	$I_L = 4.6\text{ A}, R_G = 25\ \Omega$	E_{AS}	191
Avalanche Current	I_{AS}	4.6	A
Repetitive Avalanche Energy (Note 1)	E_{AR}	1.6	mJ
MOSFET dv/dt	dv/dt	120	V/ns
Peak Diode Recovery dv/dt (Note 2)		50	
Lead Temperature for Soldering Purposes (1/8" from case for 10 seconds)	T_L	260	$^\circ\text{C}$

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

*Drain current limited by maximum junction temperature.

1. Repetitive rating: pulse-width limited by maximum junction temperature.
2. $I_{SD} \leq 11.5\text{ A}$, $di/dt \leq 200\text{ A}/\mu\text{s}$, $V_{DD} \leq 400\text{ V}$, starting $T_J = 25^\circ\text{C}$.

V_{DSS}	$R_{DS(on)}\text{ MAX}$	$I_D\text{ MAX}$
600 V	120 mΩ @ 10 V	28 A



TO-247 Long Leads
CASE 340CX

MARKING DIAGRAM



T120N60S5Z = Specific Device Code
A = Assembly Location
YWW = Data Code (Year & Week)
ZZ = Assembly Lot

ORDERING INFORMATION

Device	Package	Shipping
NTHL120N60S5Z	TO-247	30 Units / Tube

NTHL120N60S5Z

THERMAL CHARACTERISTICS

Parameter	Symbol	Value	Unit
Thermal Resistance, Junction-to-Case, Max.	$R_{\theta JC}$	0.78	°C/W
Thermal Resistance, Junction-to-Ambient, Max.	$R_{\theta JA}$	40	

ELECTRICAL CHARACTERISTICS ($T_J = 25^\circ\text{C}$ unless otherwise noted)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
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OFF CHARACTERISTICS

Drain-to-Source Breakdown Voltage	$V_{(BR)DSS}$	$V_{GS} = 0\text{ V}, I_D = 1\text{ mA}, T_J = 25^\circ\text{C}$	600	–	–	V
Drain-to-Source Breakdown Voltage Temperature Coefficient	$\Delta V_{(BR)DSS} / \Delta T_J$	$I_D = 10\text{ mA}$, Referenced to 25°C	–	630	–	mV/°C
Zero Gate Voltage Drain Current	I_{DSS}	$V_{GS} = 0\text{ V}, V_{DS} = 600\text{ V}, T_J = 25^\circ\text{C}$	–	–	1	μA
Gate-to-Source Leakage Current	I_{GSS}	$V_{GS} = \pm 20\text{ V}, V_{DS} = 0\text{ V}$	–	–	±5	μA

ON CHARACTERISTICS

Drain-to-Source On Resistance	$R_{DS(on)}$	$V_{GS} = 10\text{ V}, I_D = 11.5\text{ A}, T_J = 25^\circ\text{C}$	–	96	120	mΩ
Gate Threshold Voltage	$V_{GS(th)}$	$V_{GS} = V_{DS}, I_D = 2.2\text{ mA}, T_J = 25^\circ\text{C}$	2.4	–	4.0	V
Forward Trans-conductance	g_{FS}	$V_{DS} = 20\text{ V}, I_D = 11.5\text{ A}$	–	17.1	–	S

CHARGES, CAPACITANCES & GATE RESISTANCE

Input Capacitance	C_{ISS}	$V_{DS} = 400\text{ V}, V_{GS} = 0\text{ V}, f = 250\text{ kHz}$	–	2088	–	pF
Output Capacitance	C_{OSS}		–	35	–	
Time Related Output Capacitance	$C_{OSS(tr)}$	$I_D = \text{Constant}, V_{DS} = 0\text{ V to } 400\text{ V}, V_{GS} = 0\text{ V}$	–	547	–	
Energy Related Output Capacitance	$C_{OSS(er)}$		–	59	–	
Total Gate Charge	$Q_{G(tot)}$	$V_{DD} = 400\text{ V}, I_D = 11.5\text{ A}, V_{GS} = 10\text{ V}$	–	40	–	nC
Gate-to-Source Charge	Q_{GS}		–	9	–	
Gate-to-Drain Charge	Q_{GD}		–	11	–	
Gate Resistance	R_G	$f = 1\text{ MHz}$	–	3.5	–	Ω

SWITCHING CHARACTERISTICS

Turn-On Delay Time	$t_{d(on)}$	$V_{GS} = 0/10\text{ V}, V_{DD} = 400\text{ V}, I_D = 11.5\text{ A}, R_G = 7.5\text{ }\Omega$	–	23	–	ns
Rise Time	t_r		–	13	–	
Turn-Off Delay Time	$t_{d(off)}$		–	78	–	
Fall Time	t_f		–	3	–	

SOURCE-TO-DRAIN DIODE CHARACTERISTICS

Forward Diode Voltage	V_{SD}	$V_{GS} = 0\text{ V}, I_{SD} = 11.5\text{ A}, T_J = 25^\circ\text{C}$	–	–	1.2	V
Reverse Recovery Time	t_{RR}	$V_{GS} = 0\text{ V}, I_{SD} = 11.5\text{ A}, di/dt = 100\text{ A}/\mu\text{s}, V_{DD} = 400\text{ V}$	–	277	–	ns
Reverse Recovery Charge	Q_{RR}		–	3664	–	nC

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

TYPICAL CHARACTERISTICS

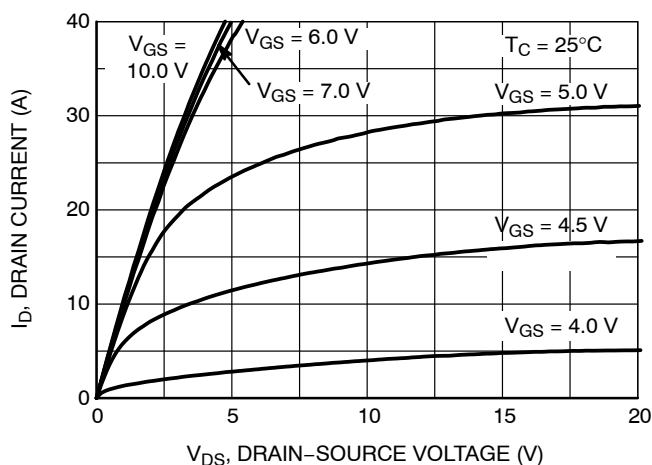


Figure 1. On-Region Characteristics

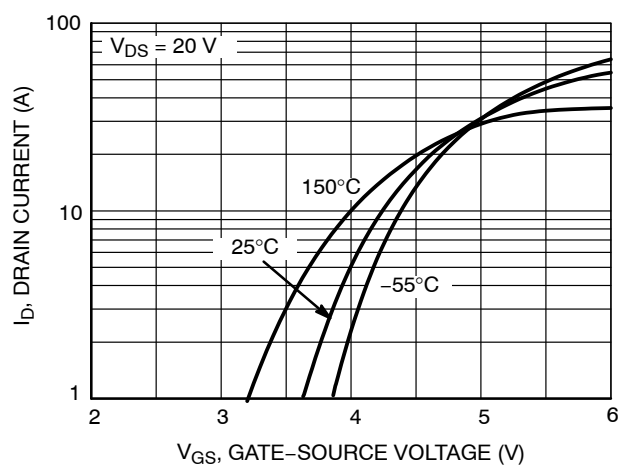


Figure 2. Transfer Characteristics

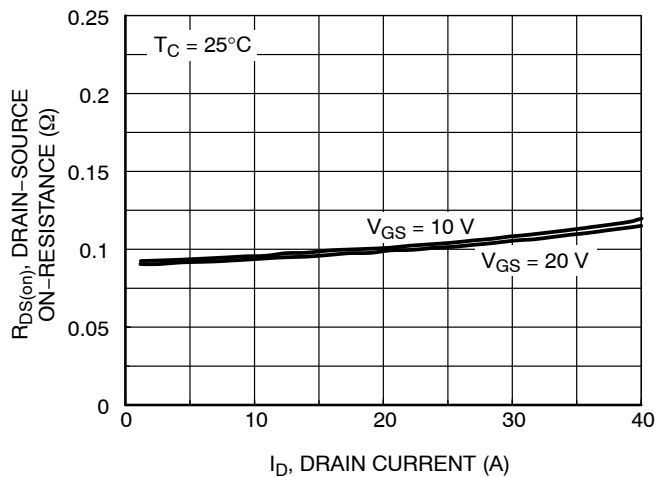


Figure 3. On-Resistance Variation vs. Drain Current and Gate Voltage

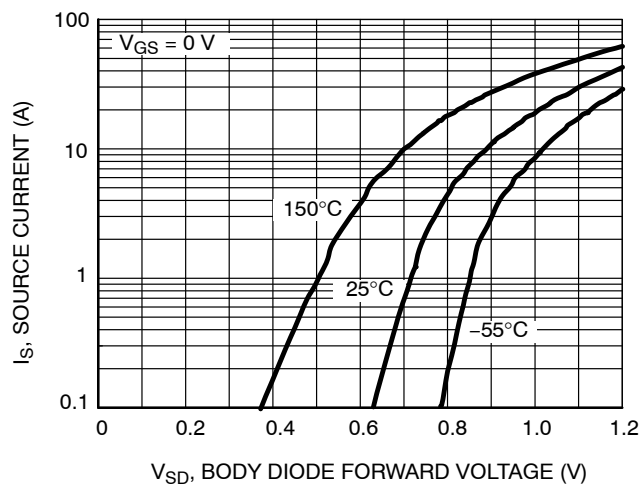


Figure 4. Body Diode Forward Voltage Variation vs. Source Current and Temperature

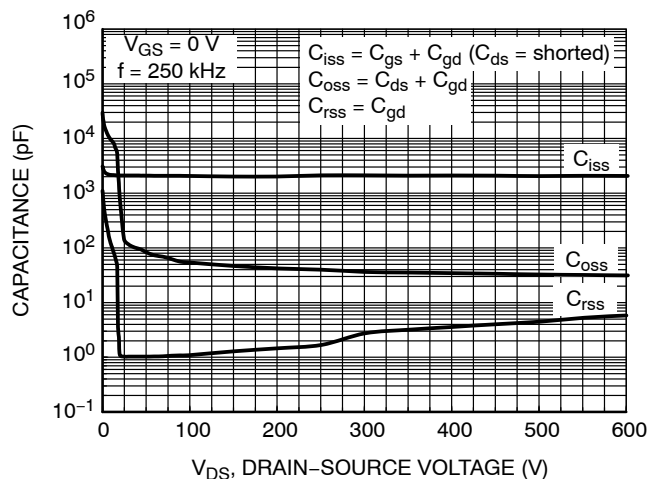


Figure 5. Capacitance Characteristics

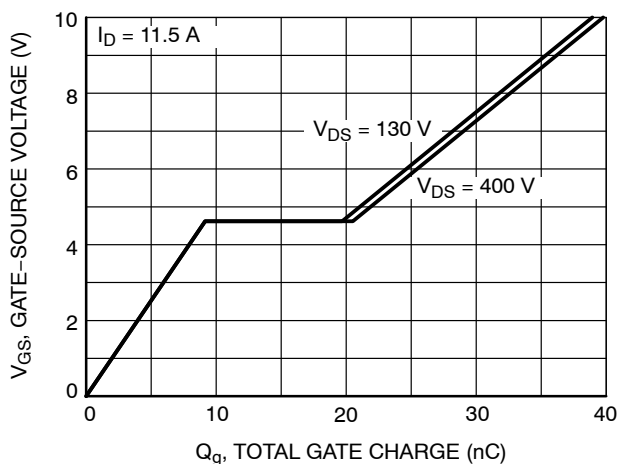


Figure 6. Gate Charge Characteristics

TYPICAL CHARACTERISTICS

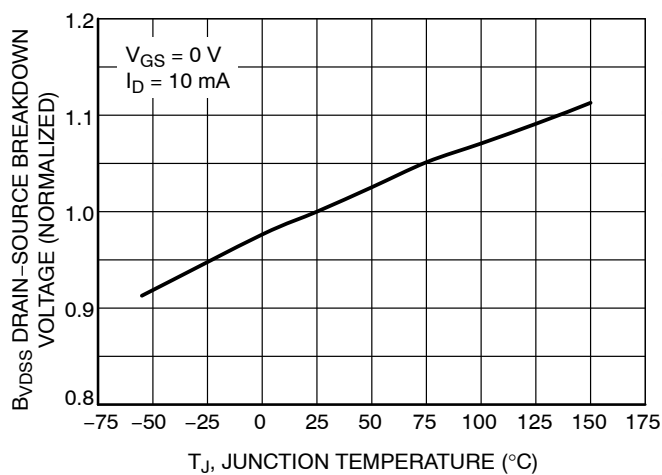


Figure 7. Breakdown Voltage Variation vs. Temperature

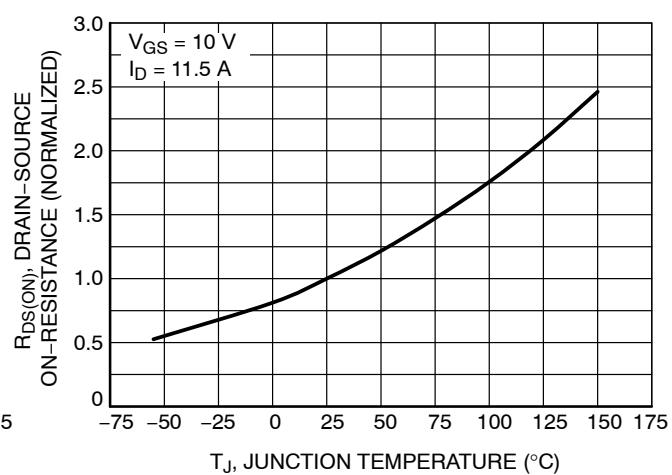


Figure 8. On-Resistance Variation vs. Temperature

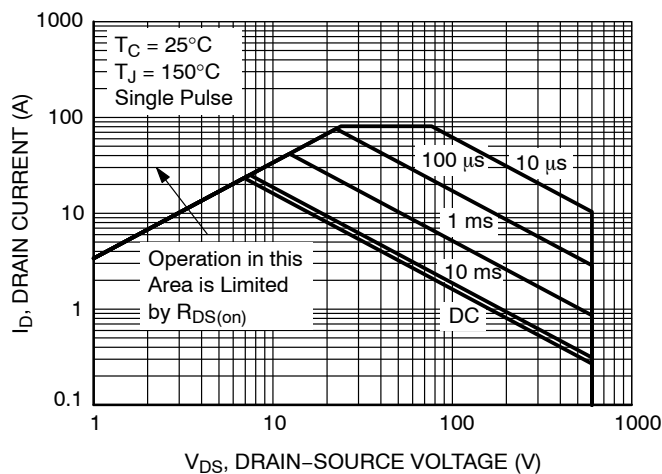


Figure 9. Maximum Safe Operating Area

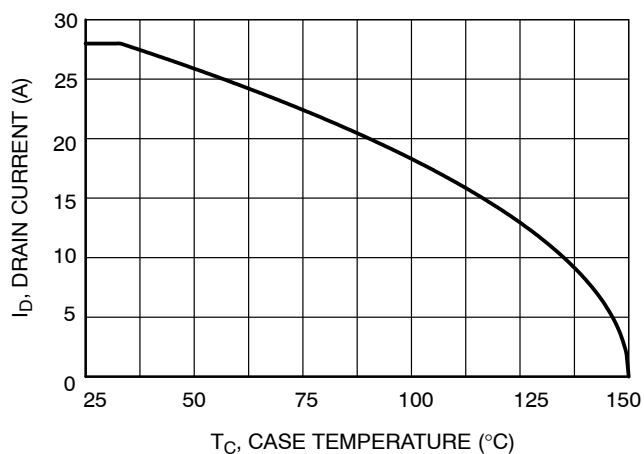


Figure 10. Maximum Drain Current vs. Case Temperature

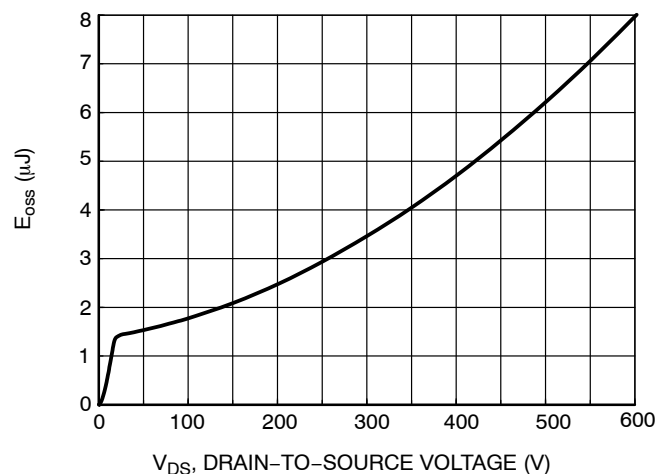


Figure 11. E_{OSS} vs. Drain to Source Voltage

NTHL120N60S5Z

TYPICAL CHARACTERISTICS

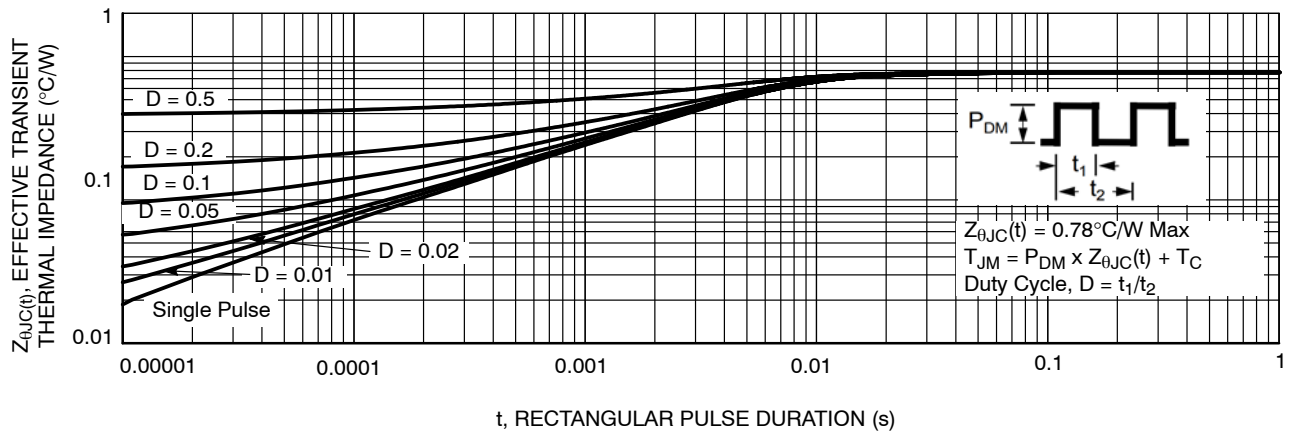


Figure 12. Transient Thermal Impedance

NTHL120N60S5Z

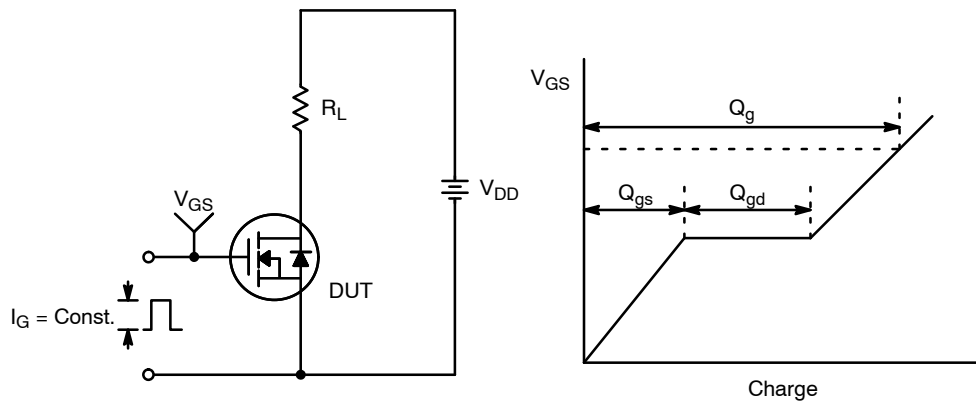


Figure 13. Gate Charge Test Circuit & Waveform

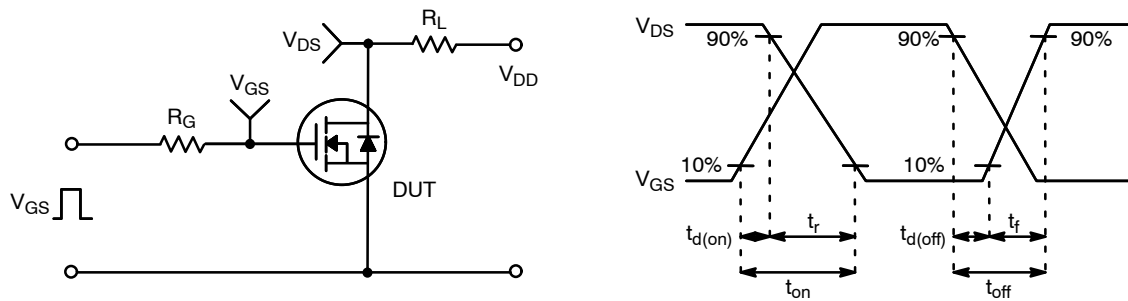


Figure 14. Resistive Switching Test Circuit & Waveforms

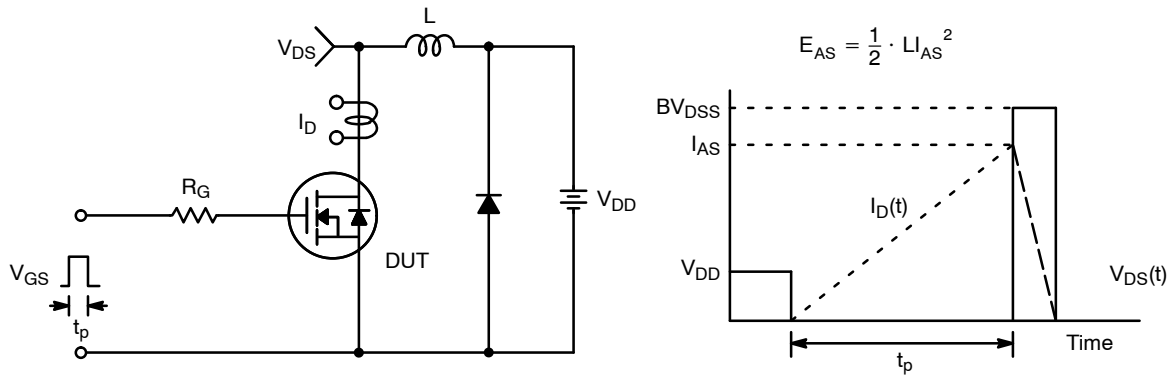


Figure 15. Unclamped Inductive Switching Test Circuit & Waveforms

NTHL120N60S5Z

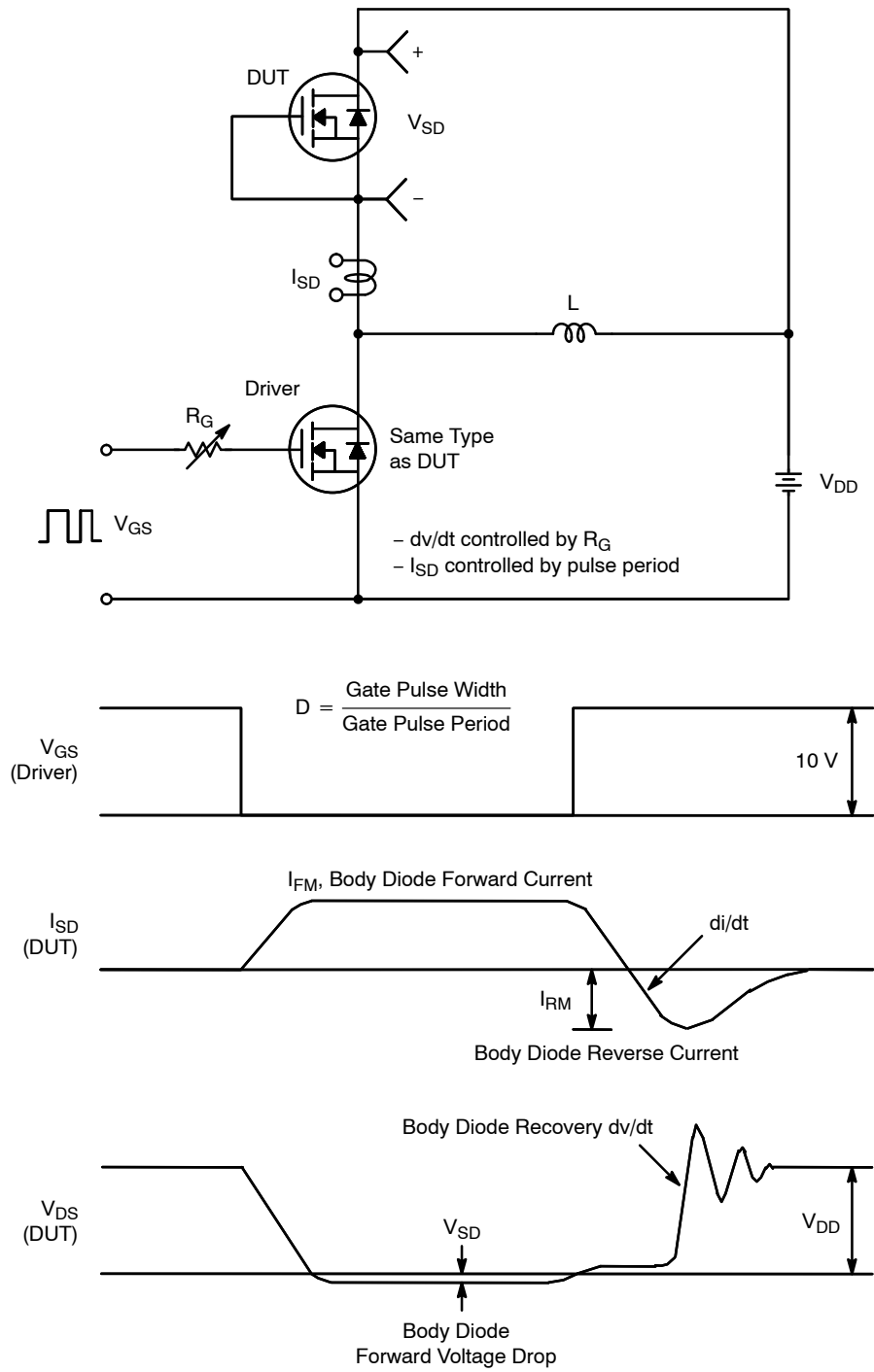


Figure 16. Peak Diode Recovery dv/dt Test Circuit & Waveforms

MECHANICAL CASE OUTLINE

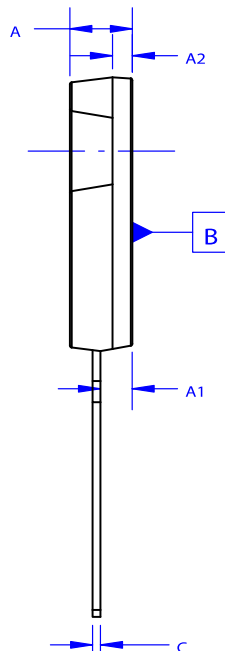
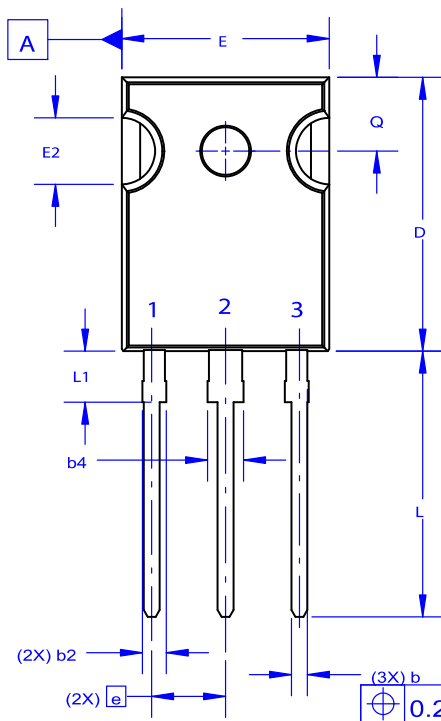
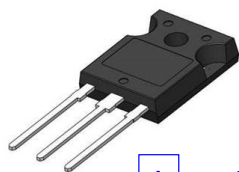
PACKAGE DIMENSIONS

ON Semiconductor®



TO-247-3LD
CASE 340CX
ISSUE A

DATE 06 JUL 2020



NOTES: UNLESS OTHERWISE SPECIFIED.

- A. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSIONS.
- B. ALL DIMENSIONS ARE IN MILLIMETERS.
- C. DRAWING CONFORMS TO ASME Y14.5 - 2009.
- D. DIMENSION A1 TO BE MEASURED IN THE REGION DEFINED BY L1.
- E. LEAD FINISH IS UNCONTROLLED IN THE REGION DEFINED BY L1.

GENERIC MARKING DIAGRAM*



XXXXX = Specific Device Code
A = Assembly Location
Y = Year
WW = Work Week
G = Pb-Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

DIM	MILLIMETERS		
	MIN	NOM	MAX
A	4.58	4.70	4.82
A1	2.20	2.40	2.60
A2	1.40	1.50	1.60
D	20.32	20.57	20.82
E	15.37	15.62	15.87
E2	4.96	5.08	5.20
e	~	5.56	~
L	19.75	20.00	20.25
L1	3.69	3.81	3.93
ØP	3.51	3.58	3.65
Q	5.34	5.46	5.58
S	5.34	5.46	5.58
b	1.17	1.26	1.35
b2	1.53	1.65	1.77
b4	2.42	2.54	2.66
c	0.51	0.61	0.71
D1	13.08	~	~
D2	0.51	0.93	1.35
E1	12.81	~	~
ØP1	6.60	6.80	7.00

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